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MANUFACTURING METHODS FOR CHROME SILICON FILM RESISTORS FOR RADIATION HARDENED CIRCUITS

G. M. Ammon
Harris Semiconductor

TECHNICAL REPORT AFML-TR-72-166

October, 1972

Air Force Materials Laboratory
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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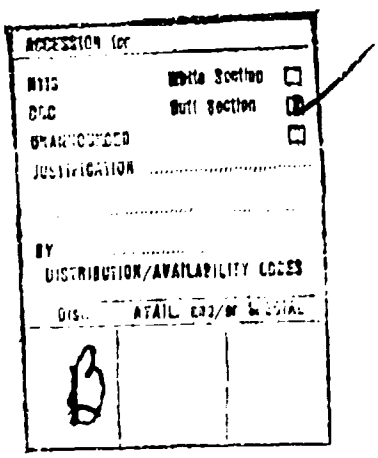

AFML-TR-72-166

MANUFACTURING METHODS FOR CHROME SILICON FILM RESISTORS FOR RADIATION HARDENED CIRCUITS

G. M. Ammon
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FOREWORD

The work described in this report was performed by Harris Semiconductor, Melbourne, Florida, for Manufacturing Methods Project Number 501-0A under Air Force Contract Number F33615-71-C-1270, dated 15 March 1971.

The Air Force project engineer for this contract was Mr. Max Bialer, AFML/LTE, Air Force Materials Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio 45433.

Mr. M. A. Weiant, Jr. was the original Harris Program Manager until the responsibility was assumed by Mr. George M. Ammon in January 1972. The chief contributors to this program and the preparation of this report were M. A. Weiant, Jr., C. J. Wredberg, C. S. Symeon, and E. M. King.

This report was submitted in July 1972 and covers work performed during the period 1 June 1971 through 1 July 1972.

Publication of this report does not constitute Air Force approval of its findings and conclusions. It is published only for the exchange and stimulation of ideas.

JULES I. WITTEBORT
Chief, Electronics Branch
Manufacturing Technology Division

ABSTRACT

The principal objective of this program was to advance the processes and techniques that are necessary to add chrome silicon thin film resistors to radiation hardened, low power integrated circuits. The applicability and repeatability of the resistor deposition techniques using AC sputtered chrome-silicide on oxidized silicon were suitable for high volume production.

The following two low power, radiation hardened transistor-transistor logic circuits were fabricated ir moderate quantities to demonstrate production readiness of the AC sputtering of thin film resistors for their use in the manufacture of radiation hardened integrated circuits.

1. Dual 4-Input Nand Gate

2. Dual D Type Flip-Flop which includes at least five resistors that have resistance value equal to or greater than 40,000 ohms.

With the successful completion in fabricating six hundred pieces of each device type and the results of severe military environmental tests on these devices, the contract objectives were satisfied.

Some of the technological areas enhanced as a result of the program included development of AC sputtered chrome silicon thin film process techniques with the following characteristics:

- Sheet resistivity of 300 to 10 kΩ per square
- Nominal resistor thicknesses of 200-300 Å
- Stability equal to or greater than nichrome resistors
- Resistor linewidth of 0.5 mil or less.

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SECTION I

INTRODUCTION

1.0 GENERAL

The objective of this project was to establish the manufacturing processes and techniques necessary to produce high resistivity thin film resistors having sheet resistivities of 1000 to 2090 ohms per square as a minimum. These resistors would be used in the design of radiation hardened, low power integrated circuits.

To this end, two logic circuits using chrome silicon thin film resistor technology were fabricated in suitable quantities to demonstrate production readiness. The circuits chosen for fabrication included a dual four input Nand gate and a Dual D clocked flip-flop.

This program was divided into two phases as follows:

- Phase I

  The purpose of this phase was to establish the processes that were suitable for the deposition of high resistivity chrome silicon thin film resistors on oxidized silicon. One hundred units of each of the two devices were to be fabricated, tested, and characterized.

- Phase II

  The purpose of this phase was to demonstrate the consistent repeatability and predictability of the chrome silicon thin film resistor processing. Five hundred units of each device were to be produced with samples of each characterized and life tested to demonstrate its reliability.

SECTION II

TECHNICAL REQUIREMENTS

2.0 GENERAL

The primary purpose of this program was to establish the manufacturing processes necessary to add high resistivity chrome silicon thin film resistors to radiation hardened, low power integrated circuits. A circuit configuration very similar to the 54L series was used as the circuit vehicle to demonstrate producibility in a production environment.

In addition to the prime specifications for the individual circuit performance, the devices were required to meet other basic environmental specifications consisting of thermal shock, life testing, operating temperature range, and nuclear environment, to name a few.

The package concept decided upon was a radiation hardened 14-lead TO-86 1/4" x 1/4".

All the preceding topics will be elaborated on in the sections to follow, beginning with:

2.1 MANUFACTURING PROCESSES

2.1.1 THIN FILM RESISTOR PROCESS

Manufacturing methods were developed to process high resistance value chrome silicon (CrSi) thin film resistors as part of an integrated circuit that would minimize the possibility of excessive resistance change and/or burnout under high-level radiation pulses.

Objective

To establish a process capable of fabricating film resistors as part of a hardened integrated circuit having the following properties:

- Sheet resistivity of 300 to 10 kΩ per square
- Temperature coefficient of resistivity of -200 to +500 parts per million per degree centigrade
- Stability equal to or better than Nichrome resistors
- Voltage coefficient such that resistance is constant above 10 μA of current
- Resistor linewidth of 0.5 mil or less

- Compatibility with silicon dioxide substrate and aluminum interconnect system
- Absolute value ±20% as a maximum
- Capable of withstanding radiation environments

2.1.2 DIELECTRIC ISOLATION

The CrSi resistor circuit vehicles used dielectric isolation processing in the place of the reverse biased junctions used in the existing micropower logic integrated circuit product line. The dielectric isolation eliminates possible latch up as a result of ionizing radiation pulses. Logic circuits were designed with only one active circuit element to each dielectrically isolated tub area (no additional active or passive elements).

2.1.3 INTERCONNECTIONS AND ASSEMBLY

An all aluminum interconnect system was used. These interconnects had maximum attainable cross section area with a minimum width of 0.5 mil except when contacting apertures. For that condition, the minimum width was 0.25 mil, and a minimum thickness of 0.7 micron. All bonding methods incorporated techniques for minimizing radiation induced bond failures thereby ensuring long life and trouble free connection under radiation, temperature cycling, vibration and other severe space type environment. Radiation hardened flatpacks were used for device packaging.

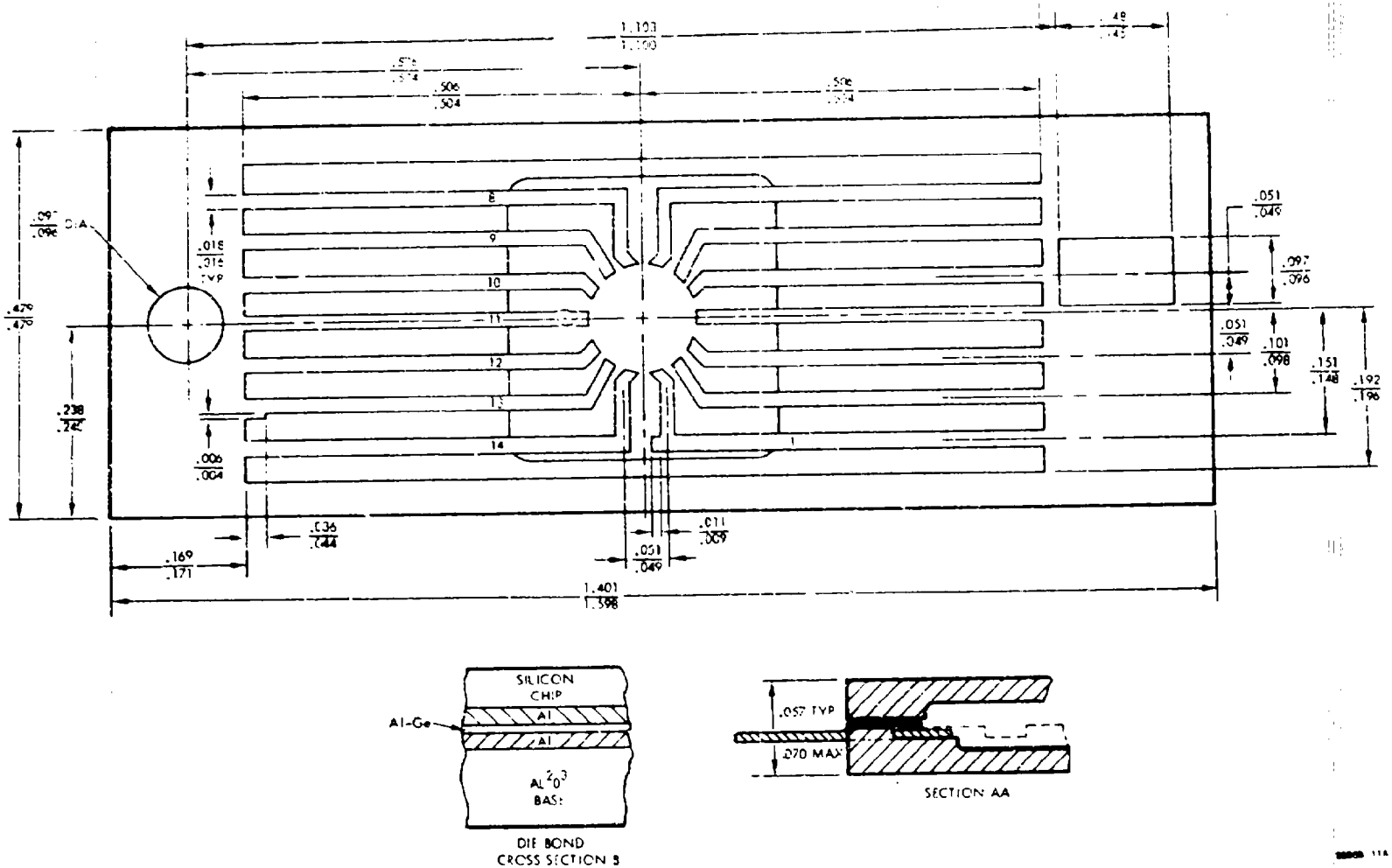
2.1.4 PACKAGE

All circuits were mounted in a 14 lead TO-86 1/4" x 1/4" radiation hardened package described below. This package is identical to the package being used for hardened logic circuits currently in production.

2.1.4.1 Package Description

The package used is shown in Figure 1. It has the following characteristics:

- The case is ceramic (94 percent Al_2O_3).
- External leads are Kovar plated with 50 to 350μ inches of gold.
- No gold, lead, or other high-atomic number material is internal to the case.
- The internal terminals are Kovar with an evaporated aluminum overcoat.
- The Al-Ge die attachment system is utilized.



DIE BOND
CROSS SECTION B

SECTION AA

Figure 1. Radiation Hardened Package TO-86

The package has passed qualification testing as specified in Figure 2. The thermal resistance between the package case and the die is less than 25° C/W.

2.1.4.2 Wire Bonding System

The wire bonding system used was an ultrasonic wire attachment with one mil aluminum wire (1 percent silicon content). The bonds at the terminals and die surface were Al-Al bonds with no high Z metals. Al-Al ultrasonic bonds produced by Harris have been extensively tested in nuclear environments without failure.

2.1.4.3 Die Attachment System

Harris has developed a die attachment technique using low Z materials. The circuit die is attached to the package using an aluminum-germanium (Al-Ge) eutectic solution. The die attach technique is a proven and reliable process. Qualification tests have been passed, as outlined in Figure 2. Microsectioning has been performed to study the wetting properties and no voiding problems have been discovered.

2.1.4.4 Package Sealing

The packages are furnace sealed using a low firing pyroceram. Leak rates of less than 1×10^{-8} cc/second-He are typical and many are below 1×10^{-9} cc/second-He.

2.2 CIRCUIT DESIGN

The two low power TTL circuits under consideration were a Dual 4-Input Nand Gate and a Dual D-Type Flip-Flop. The schematic for a basic gate is shown in Figure 3. This Nand Gate is basically identical to the 54L series with the exception of the output pullup, which was changed to a Darlington stage to improve the post-neutron performance.

2.2.1 CIRCUIT ANALYSIS

The schematics for the Dual 4-Input Gate and the Dual D-Type Flip-Flop are shown in Figures 3 and 5 with pinouts shown in Figures 4 and 6. Referring to the schematic of Figure 3, it can be seen that the major modification to a standard 54L gate is the replacement of the pullup transistor and diode with the Darlington made up of Q3 and Q4 and the resistor R5. The Darlington was chosen over a single transistor pullup to improve the post-neutron propagation delay. This results from the large value of R2 which limits the base drive to the pullup. In the case of a single transistor the output pullup current will be beta limited after the circuit has been exposed to neutron radiation doses of sufficient magnitude to greatly decrease beta. The Darlington configuration will reduce the effective RC time constant of the output risetime. Another advantage of this output

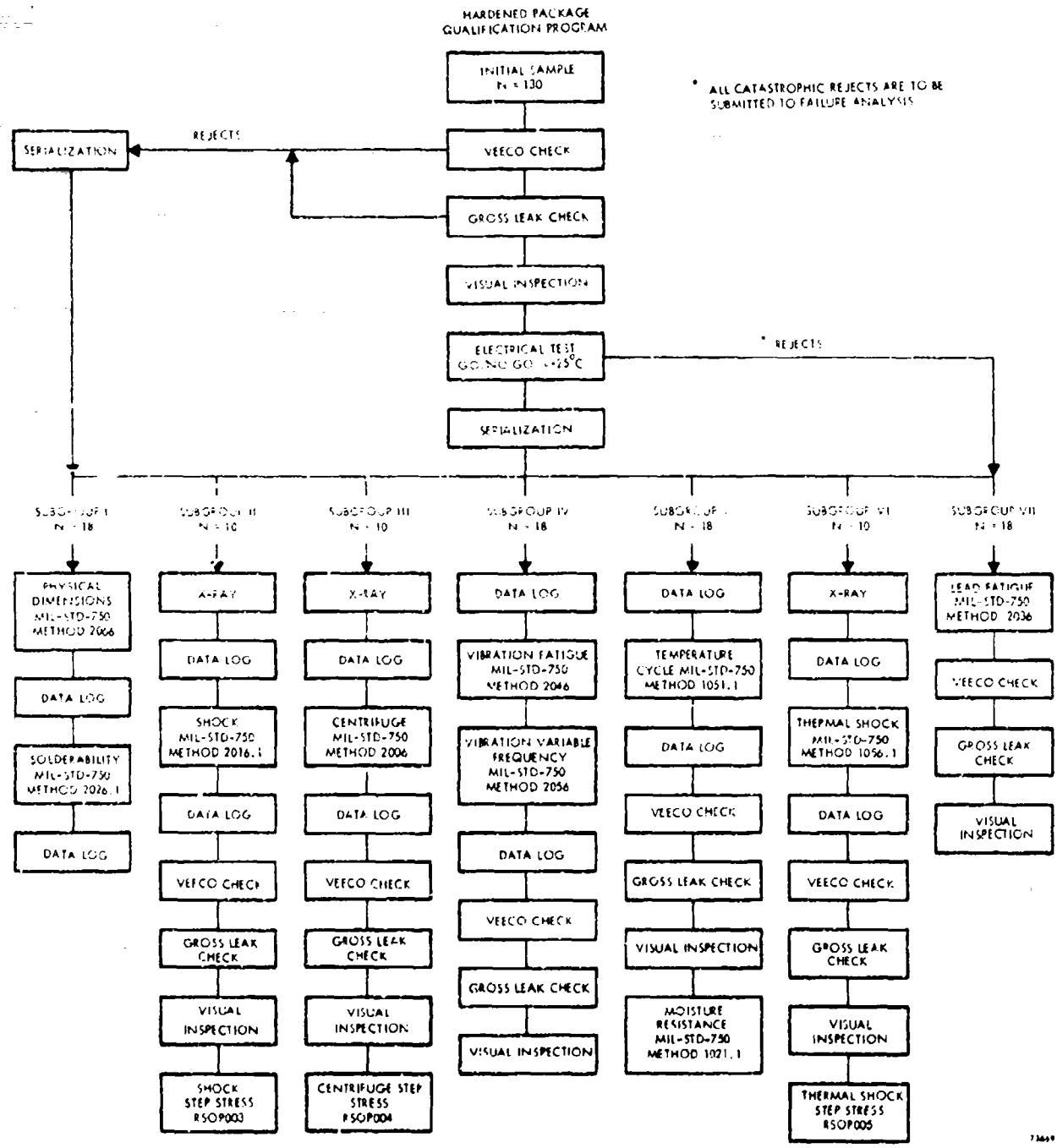


Figure 2. Hardened Package Qualification Program

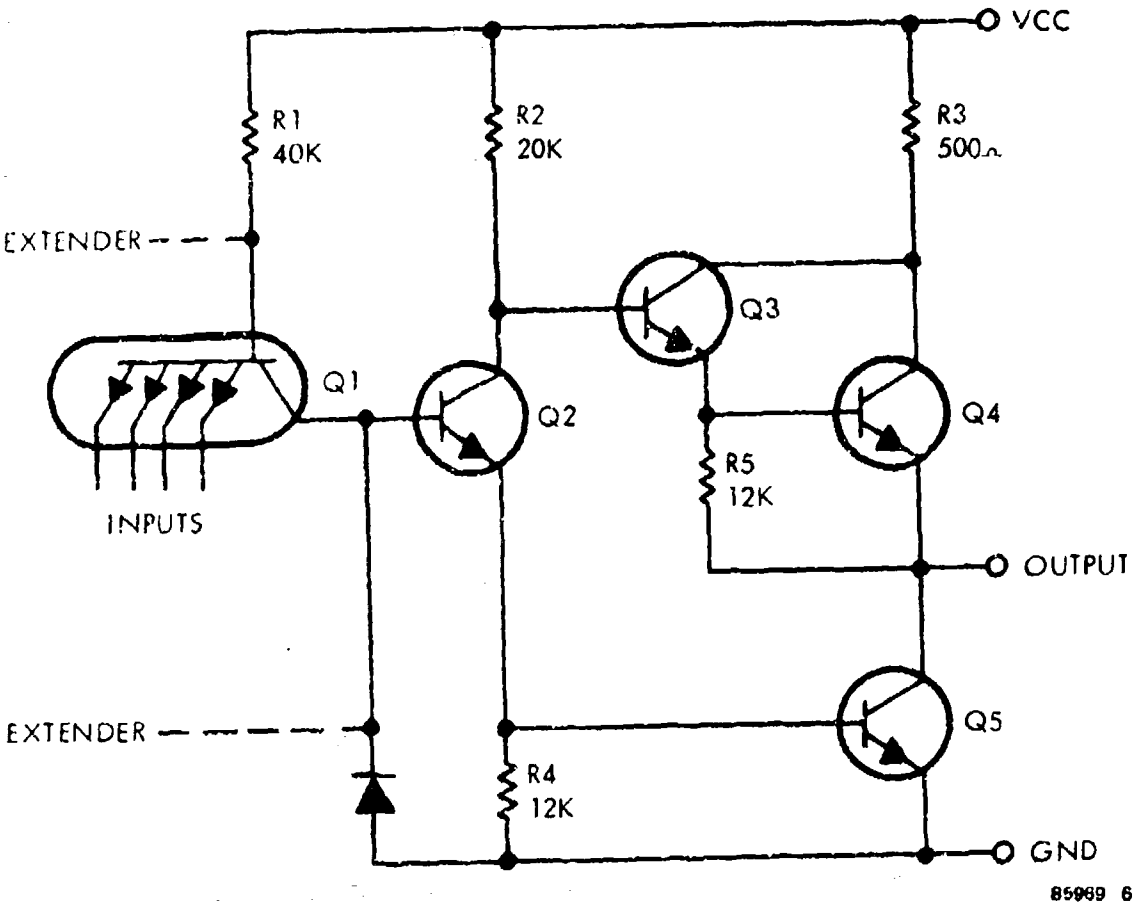


Figure 3. Dual Four Gate Schematic

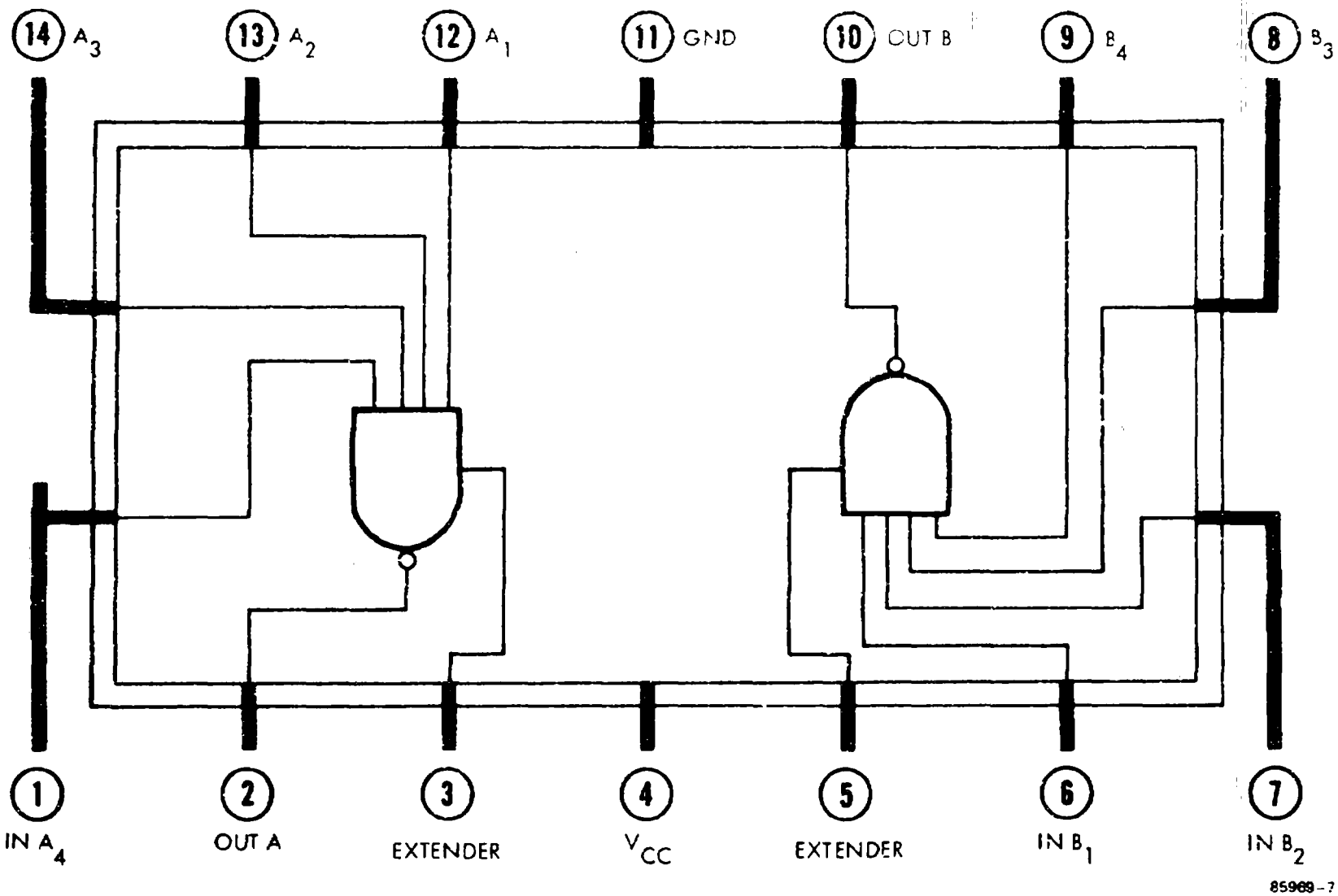


Figure 4. Dual 4-Input Gate with Extender Logic Diagram

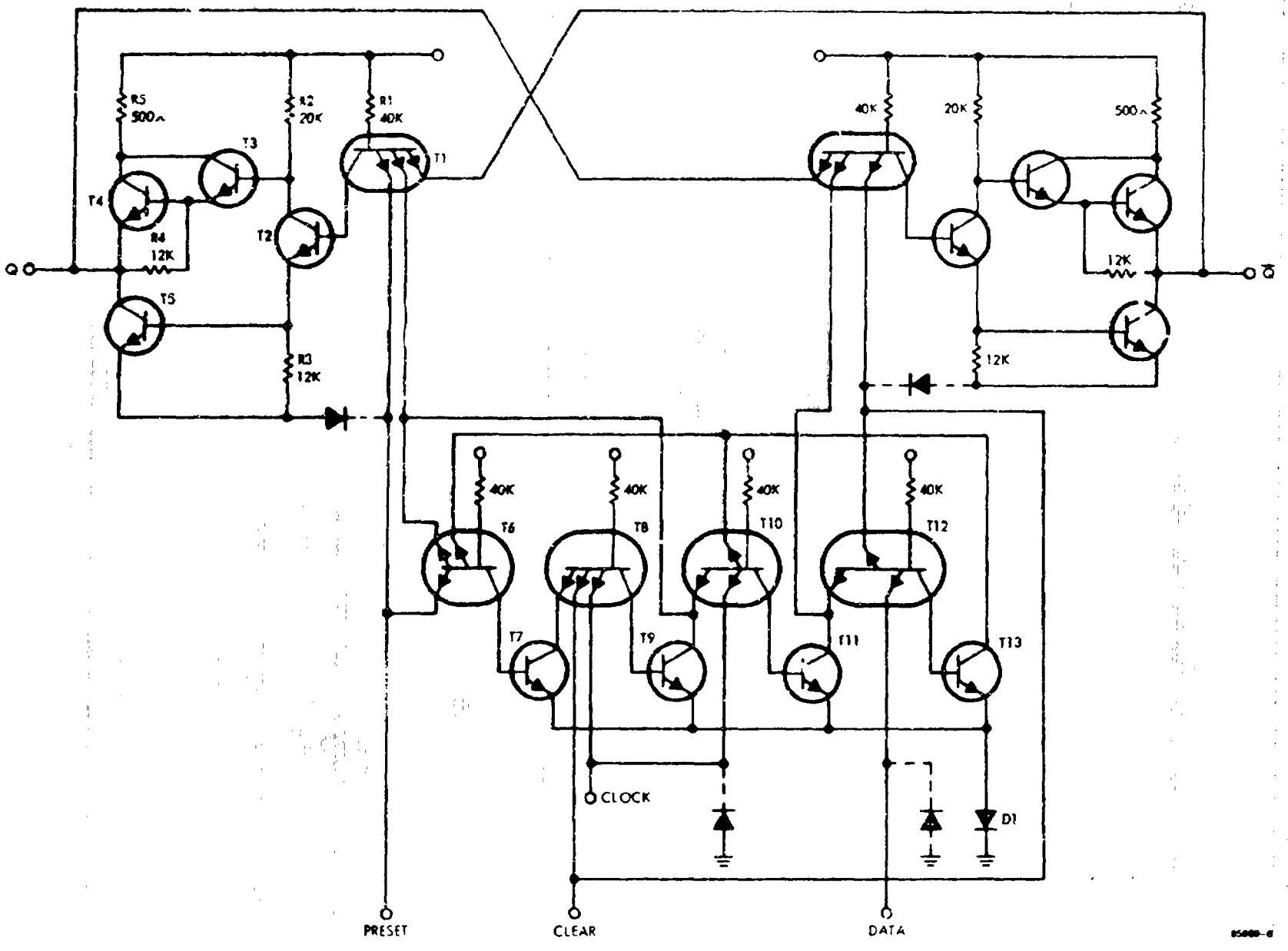


Figure 5. D-Type Flip-Flop Schematic

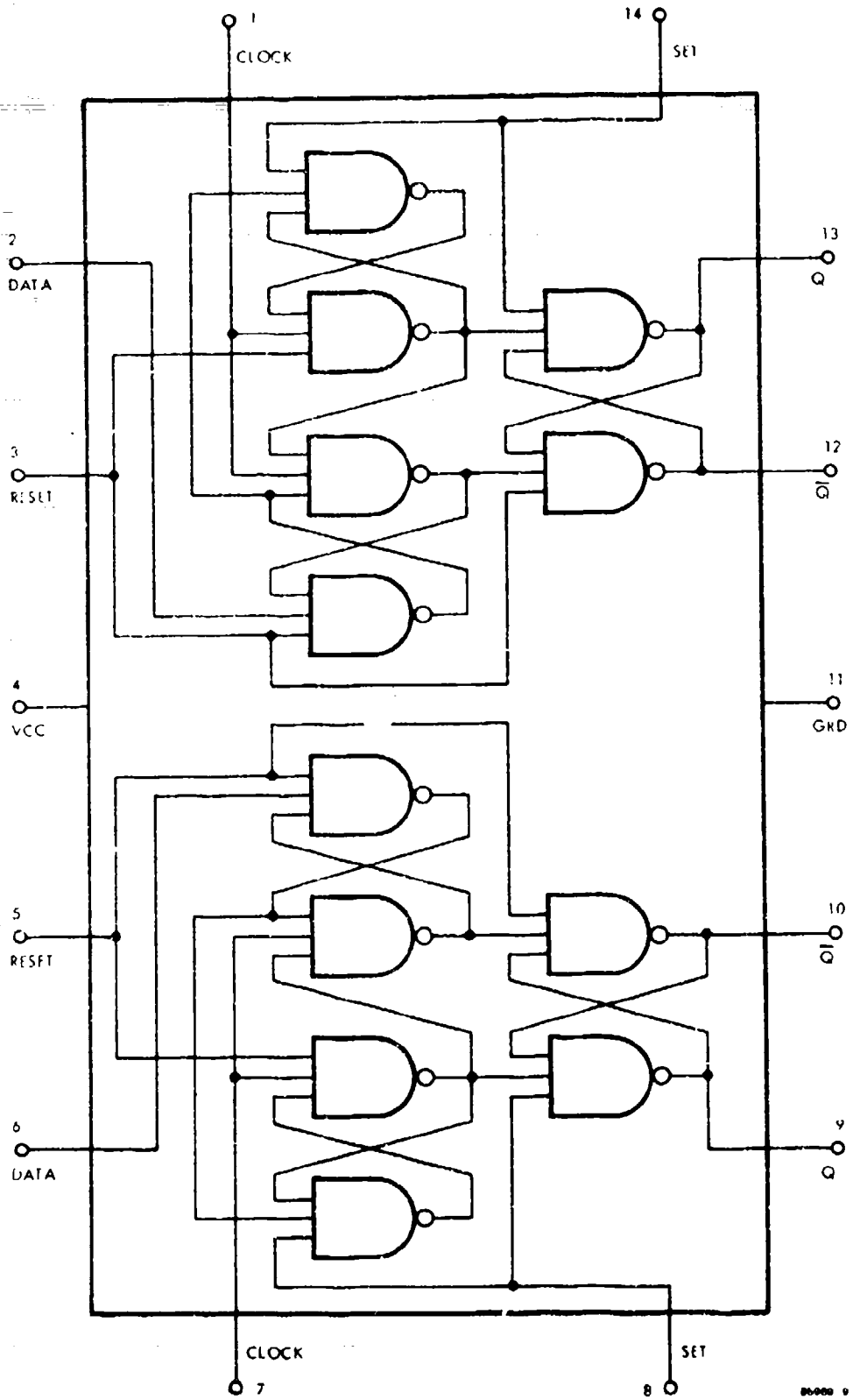


Figure 6. Dual D Flip-Flop Pinout

is an improved logical "0" threshold which results from the smaller value of base current required from R2 and the corresponding smaller voltage drop.

The resistor, R5, connected to the base of Q4 is returned to the output rather than ground to decrease power dissipation of the logical "1" state.

The disadvantages of this output pullup which are an increased component count and an increased current spike, were examined and were considered to be outweighed by the advantages.

The following is a discussion of the various performance parameters of the circuits shown in Figures 3 and 5. The electrical specifications for the 54L series were used as a starting point since they fulfilled power, speed, and performance requirements set forth in the Statement of Work.

2.2.1.1 Logical "0" Input Current

The "0" input current is determined primarily by the input resistor R1. The smaller this current, the less the current sinking capability required of the output for a constant fanout. Thus, the largest R1 consistent with speed requirements is desirable. Using a nominal value of 40 kΩ for R1, the maximum worst-case "0" input current is determined to be .15 mA. This is an improvement compared to the 54L specification of 0.18 mA.

2.2.1.2 Logical "1" Input Current

The maximum "1" input current is determined by the fanout and the maximum allowable loading of the output. This maximum "1" input current, in conjunction with the value of R1, dictates the maximum allowable inverse beta of the input transistor, Q1. For I_{IN} 1 ≤ 10$_{\mu A}$, the worst-case inverse beta must be less than 0.065.

2.2.1.3 Logical "0" Input Voltage

The minimum V_{IN} 0 threshold is derived from the maximum "0" output voltage plus the desired minimum noise margin. For V_{OUT} 0 ≤ 0.30 volt and N.M. ≥ 0.40 volt, V_{IN} 0 ≥ 0.70 volt. From this the minimum V_{BE} threshold for Q2 and Q5 and the maximum offset voltage for Q1 can be specified.

The input configuration for the flip-flop is slightly different; here V_{IN} "0" also determines the minimum V_{BE} threshold for the phase-splitter T7, minimum V_F for the common diode D1, and maximum offset voltage for the input devices.

Also, thresholds internal to the flip-flop must be considered. For the case of one input gate such as T6 and T7 driving another, such as T8 and T9, $V_{CE(SAT)}$ of the phase-splitter

T7 plus offset voltage of the input device plus 60 mV must be less than V_{BE} of the phase-splitter T8.

2.2.1.4 Logical "1" Input Voltage

The maximum V_{IN} "1" threshold was derived from the minimum "1" output voltage minus the desired minimum noise margin. Thus, V_{IN} "1" equals 2.4 volts minus 0.4 volt or 2.0 volts. From this, the maximum V_{BE} for the phase-splitter, Q2, and the output transistor, Q5, was determined.

2.2.1.5 Logical "0" Output Voltage

The maximum V_{OUT} "0" was chosen to be compatible with the 54L specifications for pre-neutron performance. Post-neutron performance will be discussed in Section 8.0. V_{OUT} "0" directly dictates the $V_{CE(SAT)}$ characteristics of the output device Q5, and the values of resistors R1, R2, and R4 which must be such that Q5 is fully saturated.

2.2.1.6 Logical "1" Output Voltage

The V_{OUT} "1" was chosen to be compatible with the 54L specifications. V_{OUT} "1" and V_{IN} "0" threshold dictates the maximum V_{BE} for Q3 and Q4 and also the maximum ratio of R2 to R4.

2.2.1.7 Output Short-Circuit Current

A maximum output short-circuit current was specified to prevent circuit damage in case of accidental shorting of the output to ground. The maximum I_{OS} determines the minimum value of R3. Switching speed with capacitive loads is the prime consideration in determining the maximum value of R3.

2.2.1.8 Power Supply Current

The Statement of Work called for a nominal power dissipation of one milliwatt per gate. For the logical "1" state, aside from leakage, all the power is dissipated in R1 and Q1 with R1 being the controlling factor, and in the logical "0" state the power is dissipated in R1 and R2. The nominal average power for one gate is 0.95 mW and 3.80 mW for one flip-flop.

2.2.1.9 Propagation Delays - t_{pd} "0", t_{pd} "1"

The Statement of Work called for a typical gate propagation delay to be in the order of 50 nanoseconds. All resistor values and the capacitances associated with Q2 and Q5 are the major determinants of propagation delays. A computer analysis was performed to predict switching speeds. The program used was SCEPTRE and the models used were derived from a previous hardened program which used a fabrication process similar to the proposed process for this contract. The computer times were pessimistic

since the model for the phase-splitter transistor Q2 has 1.9 times the base area of the phase-splitter proposed for the actual circuit and the collector-base capacitance of this device is the most important factor affecting delay times. The performance was simulated for V_{CC} = 5.0 volts, T = 25° C, and R = 1.2 $R_{NOMINAL}$ with the following results:

a. Single Nand Gate

t_{pd} "0"	27 ns
t_{pd} "1"	38 ns

b. Flip-Flop

t_{pd} "0" (Clear to Output)	65 ns
t_{pd} "1" (Clear to Output)	38 ns
t_{pd} "0" (Clock to Output)	115 ns
t_{pd} "1" (Clock to Output)	88 ns

2.2.2 ELECTRICAL PERFORMANCE SPECIFICATION

Given in Tables I and II are the electrical performance test limits and conditions. The AC test setup and the measuring conditions are shown in Figure 7.

2.2.3 RADIATION TOLERANCE LEVELS

This section will discuss the basic theoretical calculations used to predict the final radiation hardness of the end design. Both gamma and neutron radiation effects on circuit performance were evaluated.

2.2.3.1 Gamma Radiation

Both survivability and operating levels were calculated. Considering only survival, a shorted junction analysis shows all paths between V_{CC} and ground are current limited by a thin film resistor. The great majority of the shorted junction power is dissipated in R3 since it is so much smaller than R1 or R2 (reference Figure 3). The total worst-case power for R3 is 80 mW. For the Dual 4-Input Gate the total worst-case power for the package is 180 mW and for the Dual D-Type Flip-Flop it is 370 mW. These values are very safe for the chips mounted in the proposed package. Thus, the survival dose level depends on the thermomechanical characteristics of the silicon chip and the package. The two thermomechanical failure modes are melting and shock wave facturing.

Table I. Dual 4-Gate Electrical Specifications

PARAMETER	CONDITIONS[1]	PRENEUTRON		
		MIN	MAX	UNITS
I_{IN} 0 LOGICAL 0 INPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 0.3 V		0.15	mA
I_{IN} 1 LOGICAL 1 INPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 2.4 V		10	µA
	V_{CC} = 5.5 V, V_{IN} = 5.5 V		100	µA
V_{OUT} 0 LOGICAL 0 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} = 2.0 V I_{OUT} = 2 mA		0.3	VOLTS
	I_{OUT} = 1.25 mA			VOLTS
V_{OUT} 1 LOGICAL 1 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} = 0.7 V I_{OUT} = -100 µA	2.4		VOLTS
I_{OS} SHORT CIRCUIT OUTPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 0 V V_{OUT} = 0 V	-3	-15	mA
I_{CC} 0 LOGICAL 0 SUPPLY CURRENT	V_{CC} = 5.5 V, V_{IN} = 5 V		0.84	mA
t_{pd} 0 PROPAGATION DELAY TO 0 STATE	V_{CC} = 5 V, T = 25°C		60	ns
t_{pd} 1 PROPAGATION DELAY TO 1 STATE	V_{CC} = 5 V, T = 25°C		60	ns

NOTES: 1. TEMPERATURE RANGE IS -55°C TO +125°C UNLESS OTHERWISE SPECIFIED.

2. LIMIT IS 75 ns ON GATE ASSOCIATED WITH EXTENDER INPUTS.

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Table II. Dual D Flip-Flop Electrical Specifications

PARAMETER	CONDITIONS[1]	PRENEUTRON		
		MIN	MAX	UNITS
I_{IN} 0 LOGICAL 0 INPUT CURRENT[2]	V_{CC} = 5.5 V, V_{IN} = 0.3 V		0.15	mA
I_{IN} 1 LOGICAL 1 INPUT CURRENT[2]	V_{CC} = 5.5 V, V_{IN} = 2.4 V		10	µA
	V_{CC} = 5.5 V, V_{IN} = 5.5 V		100	µA
V_{OUT} 0 LOGICAL 0 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} 2.0 V			
	I_{OUT} = 2 mA		0.3	VOLTS
	I_{OUT} = 1.25 mA			VOLTS
V_{OUT} 1 LOGICAL 1 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} 0.7 V			
	I_{OUT} = -100 µA	2.4		VOLTS
I_{OS} SHORT CIRCUIT OUTPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 0 V			
	V_{OUT} = 0 V	-3	-15	mA
I_{CC} 0 LOGICAL 0 SUPPLY CURRENT	V_{CC} = 5.5 V NOTE 3		2.4	mA
t_{pd} 0 PROPAGATION DELAY TO 0 STATE	V_{CC} = 5 V, T = 25°C		150	ns
t_{pd} 1 PROPAGATION DELAY TO 1 STATE	V_{CC} = 5 V, T 25°C		100	ns

NOTES: 1. TEMPERATURE RANGE IS -55°C TO +125°C UNLESS OTHERWISE SPECIFIED.

2. FOR THE DATA, CLOCK, SET, AND RESET INPUTS USE 1, 2, 2 AND 3 RESPECTIVELY AS THE LOADING FACTOR.

3. I_{CC} IS MEASURED WITH D, CLOCK, AND SET AT GND; THEN WITH D, CLOCK AND RESET AT GND.

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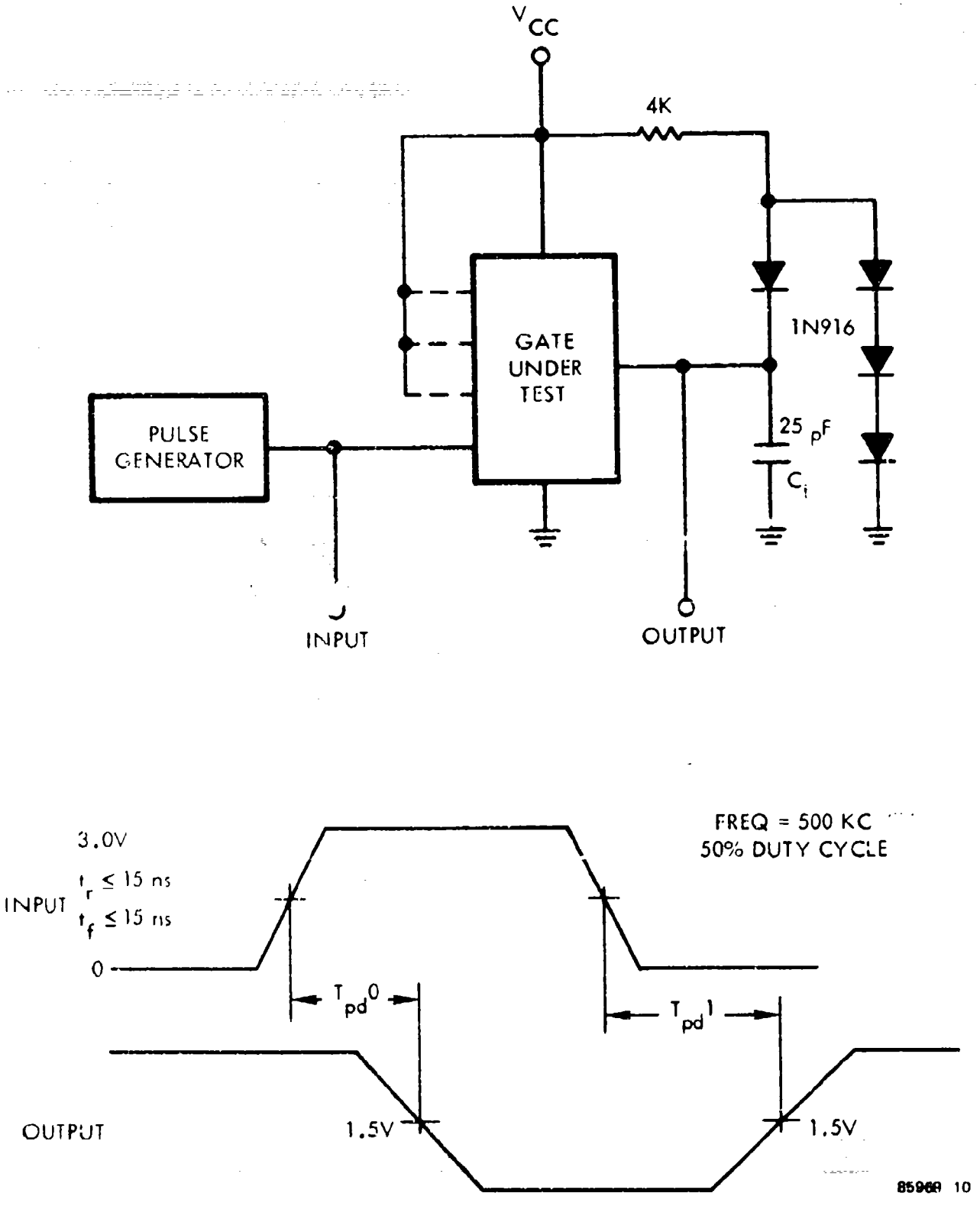

Figure 7. Switching Waveforms

Using techniques to minimize thermomechanical effects in the packaging system, the gamma dose survival level is predicted to be greatly in excess of 10^{11} rads/sec.

For operating failure levels of gamma radiation both the failure in the logical "0" state and the failure in the logical "1" state were calculated. In the "0" state, failure occurs when photocurrent generated in the base-collector depletion region turns on Q4 which pulls Q5 out of saturation. Assuming V_{OUT} = 0.7 volt is the output failure level and this occurs when $I_{E_{Q4}} \simeq 1$ mA, then the photocurrent at which failure occurs is:

$$I_{PP} = \frac{V_{BE_{Q4}}}{R5} + \frac{I_{E_{Q4}}}{\beta + 1}$$

For nominal resistor values the gamma failure rate occurs at 2×10^9 rads/sec. For worst-case, it is 1.45×10^9 rads/sec.

In the "1" state, the failure occurs when photocurrent turns on Q5, which pulls the output voltage below 2.0 volts, which occurs when $I_{C_{Q5}} \simeq 2.5$ mA. This corresponding photocurren is:

$$I_{PP} = \frac{V_{BE_{Q5}}}{R4} + \frac{I_{C_{Q5}}}{\beta}$$

which occurs at 2.9×10^9 rads/sec for nominal resistors and at 1.8×10^9 rads/sec for worst-case resistors.

One other consideration is the increased V_{OUT} load caused by photocurrent generated in the emitter-base junctions of the input device Q1. This I_{PP} was calculated to be 18 μA for a gamma level of 4×10^9 rads/sec. Thus, for a fanout of ten, the increase in the V_{OUT} "1" load could be 180 μA or a total of 280 μA. This is insignificant.

2.2.3.2 Neutron Radiation

The primary result of neutron irradiation is the degradation of forward current gain of the transistor. Circuit failure occurs when this decreasing beta causes the output transistor Q5 to come out of saturation since the base drive remains constant and the collector current remains constant until the output fails. In calculating the following failure levels, a final beta of 1.15 times the forced beta was considered necessary to prevent failure. Thus, the failure level occurs when:

$$\beta_{FINAL} \leq 1.15\, \beta_{FORCED} = 1.15\, \frac{I_C}{I_B}$$

Also $$\frac{\beta_{INITIAL}}{\beta_{FINAL}} = 1 + \frac{\tau_i \phi}{K}$$

where $\beta_{INITIAL}$ = pre-neutron current gain

β_{FINAL} = post-neutron current gain

τ_i = pre-neutron lifetime

ϕ = neutron fluence

K = damage constant

Calculating the forced beta and using these equations with τ_i = 2.5 ns and K = 2.8 x 10^5, ϕ will be calculated for a nominal and a worst-case.

For the nominal case:

T = 25° C

V_{CC} = 5.0 V

I_C = 10 x (I_{IN}) nominal) = 1.0 mA

V_{OUT} "0" = 0.5 V

Resistors = Nominal values

β_i = 50

This gives β_{FINAL} = 1.15 β_{FORCED} = 5.4

and ϕ = 9.2 x 10^{14} neutrons/cm^2

For the worst-case:

T = -55° C

V_{CC} = 4.5 V

I_C = 1.25 mA

V_{OUT} "0" = 0.4 V

Resistors = Nominal + 20%

β_i = 45

This gives $\beta_{FINAL} = 1.15\ \beta_{FORCED} = 12.6$ @ -55° C

$\beta_{FINAL} = 23$ @ $+25^{\circ}$ C

and $\phi = 1.07 \times 10^{14}$ neutrons/cm^2

Thus, the circuits predicted to have immunity to neutron irradiation up 10^{14} neutrons/cm^2.

2.2.3.3 Electrical Performance

2.2.3.3.1 Parametric Performance

Tables III and IV tabulate the calculated comparison of pre- and post-neutron electrical performance test conditions and limits. Post-neutron refers to times greater than the fast annealing time after neutron irradiation of 10^{14} neutrons per cm^2.

2.2.3.3.2 Propagation Delays

As pointed out in Paragraph 2.2.1.9, a computer analysis was performed to predict switching speeds. Following is a tabulation of the comparison of the pre- and post-neutron performance as predicted from the simulated program. The conditions used to simulate the operation were $V_{CC} = 5.0$ volts, $T = 25^{\circ}$ C and $R = 1.2\ R_{NOMINAL}$.

Single Nand Gate	Pre-Neutron	Post-Neutron
t_{pd} "0"	27 ns	34 ns
t_{pd} "1"	38 ns	39 ns
Flip-Flop	**Pre-Neutron**	**Post-Neutron**
t_{pd} "0" (Clear to Output)	65 ns	73 ns
t_{pd} "1" (Clear to Output)	38 ns	39 ns
t_{pd} "0" (Clock to Output)	115 ns	137 ns
t_{pd} "1" (Clock to Output)	88 ns	103 ns

2.3 GENERAL SPECIFICATIONS

In addition to fulfilling the process and circuit requirements, the circuit devices also had to meet all the following environmental and performance specifications.

Table III. Dual 4-Gate Electrical Specifications

PARAMETER	CONDITIONS[1]	PRENEUTRON		POSTNEUTRON		
		MIN	MAX	MIN	MAX	UNITS
I_{IN} 0 LOGICAL 0 INPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 0.3 V		0.15		0.15	mA
I_{IN} 1 LOGICAL 1 INPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 2.4 V		10		10	µA
	V_{CC} = 5.5 V, V_{IN} = 5.5 V		100		100	µA
V_{OUT} 0 LOGICAL 0 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} = 2.0 V					
	I_{OUT} = 2 mA		0.3			VOLTS
	I_{OUT} = 1.25 mA				0.3	VOLTS
V_{OUT} 1 LOGICAL 1 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} = 0.7 V					
	I_{OUT} = -100 µA	2.4		2.4		VOLTS
I_{OS} SHORT CIRCUIT OUTPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 0 V					
	V_{OUT} = 0 V	-3	-15	-3	-15	mA
I_{CC} 0 LOGICAL 0 SUPPLY CURRENT	V_{CC} = 5.5 V, V_{IN} = 5 V		0.84		0.84	mA
t_{pd} 0 PROPAGATION DELAY TO 0 STATE	V_{CC} = 5 V, T = 25°C		60		70	ns
t_{pd} 1 PROPAGATION DELAY TO 1 STATE	V_{CC} = 5 V, T = 25°C		60		65	ns

NOTES: 1. TEMPERATURE RANGE IS -55°C TO +125°C UNLESS OTHERWISE SPECIFIED.

2. LIMIT IS 75 ns ON GATE ASSOCIATED WITH EXTENDER INPUTS.

3. LIMIT IS 85 ns ON GATE ASSOCIATED WITH EXTENDER INPUTS.

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Table IV. Dual D Flip-Flop Electrical Specifications

PARAMETER	CONDITIONS[1]	PRENEUTRON		POSTNEUTRON		
		MIN	MAX	MIN	MAX	UNITS
I_{IN} 0 LOGICAL 0 INPUT CURRENT[2]	V_{CC} = 5.5 V, V_{IN} = 0.3 V		0.15		0.15	mA
I_{IN} 1 LOGICAL 1 INPUT CURRENT[2]	V_{CC} = 5.5 V, V_{IN} = 2.4 V		10		10	µA
	V_{CC} = 5.5 V, V_{IN} = 5.5 V		100		100	µA
V_{OUT} 0 LOGICAL 0 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} 2.0 V					
	I_{OUT} = 2 mA		0.3			VOLTS
	I_{OUT} = 1.25 mA				0.3	VOLTS
V_{OUT} 1 LOGICAL 1 OUTPUT VOLTAGE	V_{CC} = 4.5 V, V_{IN} 0.7 V					
	I_{OUT} = -100 µA	2.4		2.4		VOLTS
I_{OS} SHORT CIRCUIT OUTPUT CURRENT	V_{CC} = 5.5 V, V_{IN} = 0 V					
	V_{OUT} = 0 V	-3	-15	-3	-15	mA
I_{CC} 0 LOGICAL 0 SUPPLY CURRENT	V_{CC} = 5.5 V NOTE 3		2.4		2.4	mA
t_{pd} 0 PROPAGATION DELAY TO 0 STATE	V_{CC} = 5 V, T = 25°C		150		160	ns
t_{pd} 1 PROPAGATION DELAY TO 1 STATE	V_{CC} = 5 V, T = 25°C		100		115	ns

NOTES. 1. TEMPERATURE RANGE IS -55°C TO +125°C UNLESS OTHERWISE SPECIFIED.

2. FOR THE DATA, CLOCK, SET AND RESET INPUTS USE 1, 2, 2 AND 3 RESPECTIVELY AS THE LOADING FACTOR.

3. I_{CC} IS MEASURED WITH D, CLOCK, AND SET AT GND; THEN WITH D, CLOCK AND RESET AT GND.

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2.3.1 ENVIRONMENTAL SPECIFICATIONS

2.3.1.1 Temperature Range

The process was to satisfy performance requirements herein over the temperature range of -55° C to +125° C. The nonoperating storage temperature range of the low power logic devices was -65° C to +150° C.

2.3.1.2 Nuclear Environment

The circuits including the resistors were to be immune to permanent degradation from neutron irradiation at 10^{13} neutrons/cm^2, (1 Mev energy equivalent), with immunity up to 10^{14} neutrons/cm^2 if this does not interfere with other desirable characteristics of the devices. Established techniques and manufacturing methods were to be used to eliminate possibility of induced latch up and ensure high quality, reliable devices.

2.3.2 PERFORMANCE

The low power integrated logic circuit vehicles must satisfy the performance requirements herein.

2.3.2.1 Supply Voltage

The devices shall have a single power supply voltage of 5 volts nominal, 4.5 volts to 5.5 volts range.

2.3.2.2 Power

At fifty percent duty cycle, typical power drains of the logic circuits will not exceed one milliwatt per gate and less than four milliwatts for the clocked flip-flop.

2.3.2.3 Speed

Typical gate propagation delay time is to be in the order of 50 nanoseconds. The binary clock rates will be approximately 2.5 MHz.

2.3.2.4 Noise

The noise immunity shall be as great as practical in order to minimize the effect of radiation induced transient signals. Over the environmental and voltage range specified herein, the DC noise margins will not fall below 400 millivolts. The units will be designed to provide low AC noise susceptibility.

2.3.2.5 Logic Levels

It was expected that the output logic level would be 2.4 volts or larger for an input level that would not exceed

700 millivolts, and that the output logic would not exceed 300 millivolts for input voltages of 2 volts or greater.

2.3.2.6 Fanout

The minimal fanout for one low power, medium speed, integrated logic gate will be 10.

SECTION III

DEVICE DESIGN

3.0 GENERAL

The following sections discuss the wafer fabrication processes including device geometries, material specifications and diffusion profiles. The primary considerations for a producible device design were electrical performance, immunity to irradiation, and acceptable yields.

3.1 DEVICE GEOMETRIES

In Figure 8, typical device geometries are given for the phase-splitter and output devices. Figure 9 shows two types of input devices. Electrical performance requirements suggest a minimum geometry for the phase-splitter. Thus, this device geometry was made as small as possible without sacrificing fabrication yields. Electrical performance, specifically logical "0" input voltage requirements, dictated the output device, Q5, geometry. The primary consideration for the input device was a tradeoff between offset voltage and inverse beta which resulted from the input voltage thresholds and logical "1" input current requirements. The input device geometry was changed for various circuit inputs in order to facilitate the layout. Following is a list of the diffusion layout ground rules used:

- Alignment mark tolerance (masking) = .05 mil
- Minimum apertures = 0.3 x 0.3 mil^2 or 0.25 x 0.4 mil^2
- Emitter aperture to emitter diffusion = 0.15 mil
- Emitter diffusion to base diffusion = 0.15 mil
- Emitter diffusion to base aperture = 0.4 mil
- Base diffusion to collector contact = 0.3 mil

The following were minimum layout ground rules used for metal interconnect.

- Metal width = 0.4 mil
- Metal separation = 0.4 mil
- Metal aperture overlap = 0.1 mil
- Sheet resistivity = 0.028 ohm per square

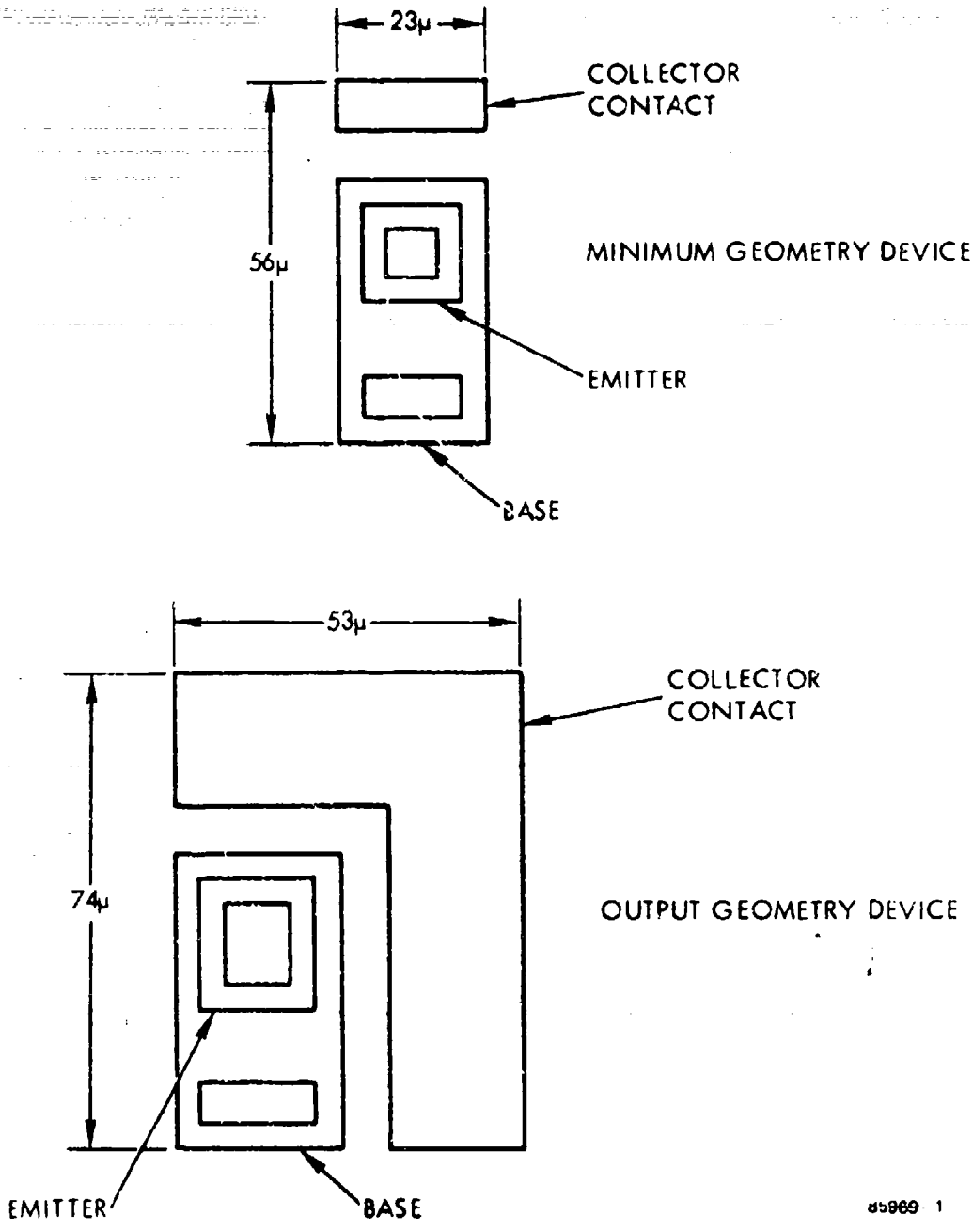


Figure 8. Transistor Geometries

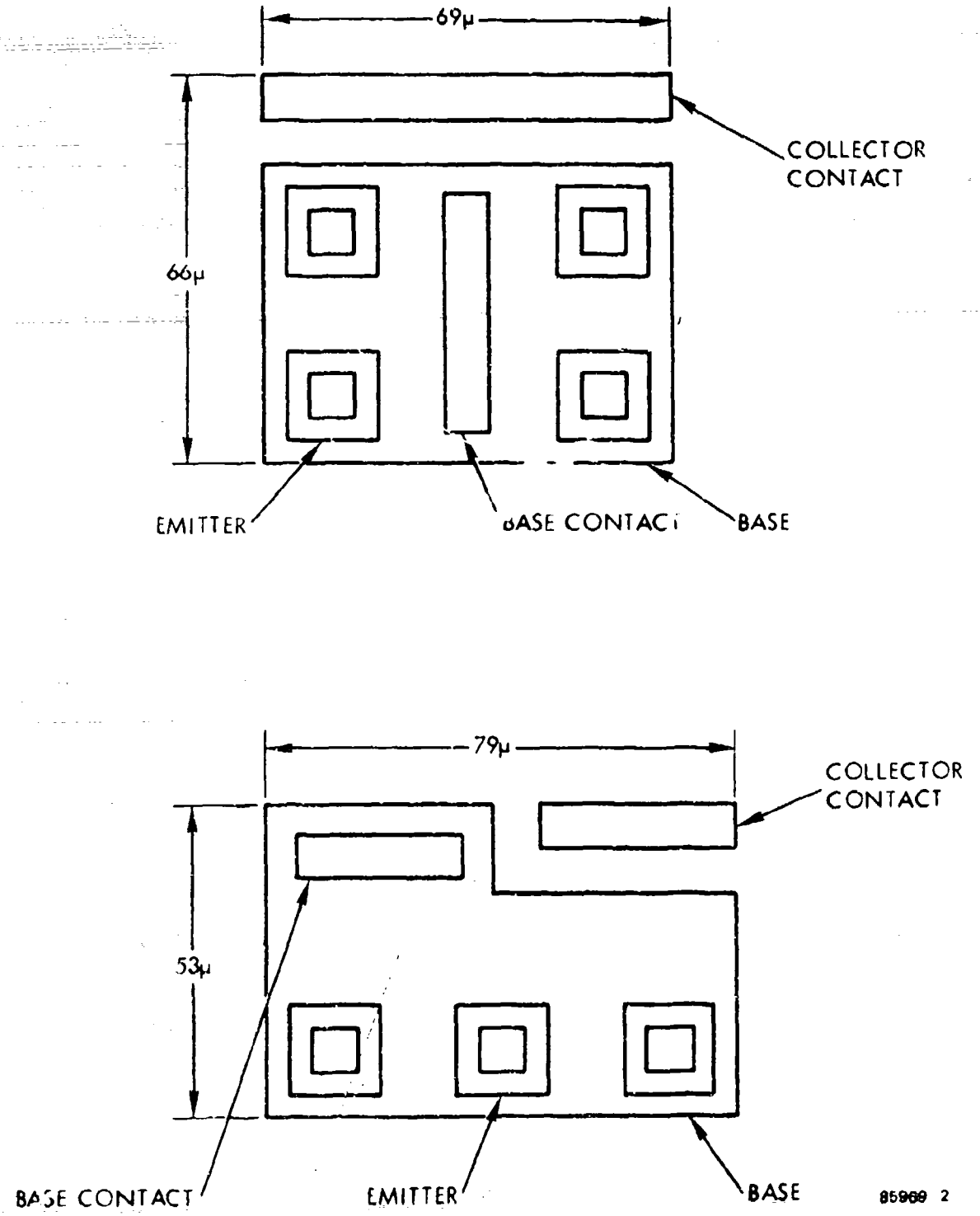


Figure 9. Input Transistor Geometries

3.2 MATERIAL SPECIFICATIONS AND DIFFUSION PROFILES

The starting wafer had single-crystalline silicon islands, each isolated electrically through the use of silicon dioxide. The fabrication techniques had been developed to the extent that routine production methods furnished the controls necessary for volume production of this dielectrically isolated material. The starting material conformed to the following specifications:

- Type — N, 2"
- Resistivity — 0.13 ohm-cm
- N-collector thickness — 0.50 mil
- N+ Epi thickness — 0.30 mil
- N+ resistivity — 0.004 ohm-cm

The base sheet target was 115 - 135 ohms per square. The base penetration was 2.1 to 2.4 microns with the base width 0.6 micron or less.

A protective overcoat of 10,000 Å of silox (SiO_2) was deposited on each slice prior to scribing.

3.3 DEVICE PARAMETERS

A typical device cross-section is shown in Figure 10. Using the geometries shown in Paragraph 3.1, the following device parameters were calculated. The device parameters and their conditions are those determined in Paragraph 2.2.1 to be necessary for the circuits to meet the electrical performance specifications.

3.3.1 INPUT DEVICE Q1

Parameter		
BV_{CBO}, I_C	= 100 μA	>25 V
BV_{CEO}, I_C	= 5 mA	>7 V
BV_{EBO}, I_E	= 100 μA	>6.5 V
H_{FE}, I_C	= 100 μA	>5
β_{EE}, I_E	= 10 μA at 125° C	<.02
V_{OFFSET}, I_B	= 100 μA at 125° C	<150 mV
C_{OB}, V_{CB}	= 2.5 V	<1.2 pF

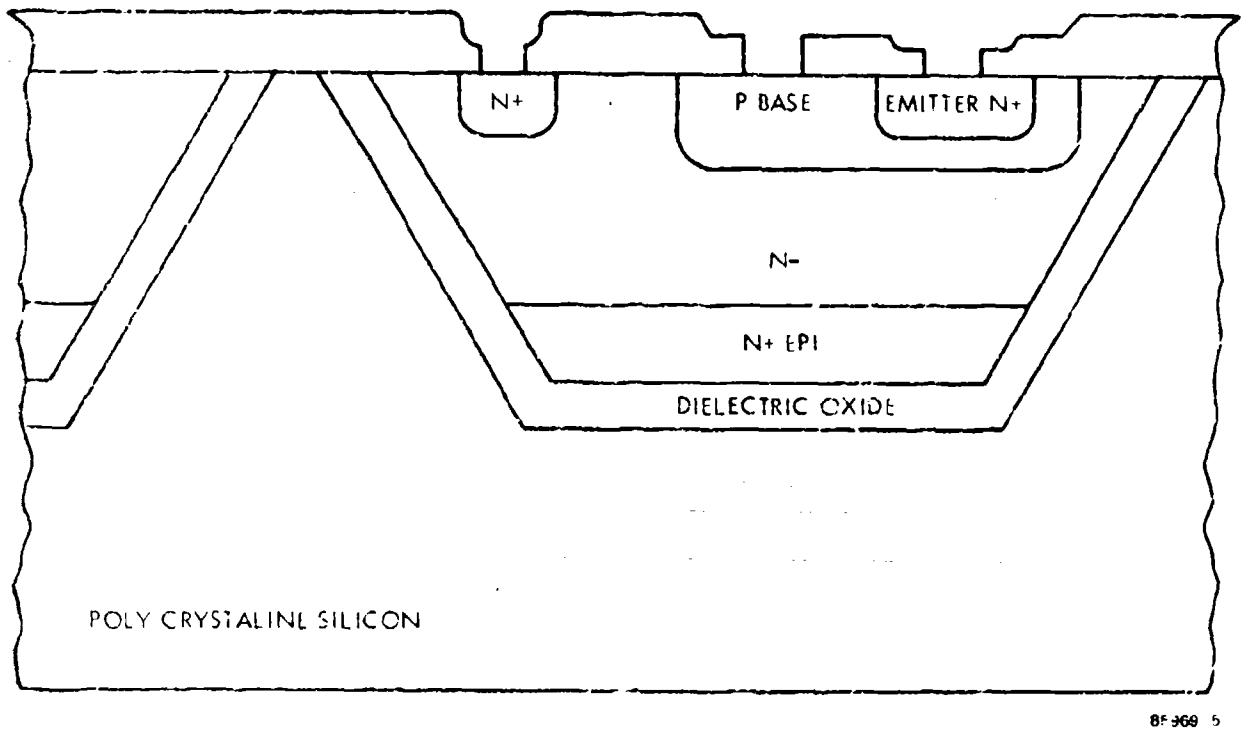


Figure 10. Device Cross-Section

C_{IB}, V_{BE}	= 0.5 V	<0.5 pF
I_{PP}, V_{CB}	= 2.5 V	= 10 x $10^{-8}\dot{\gamma}\mu A$
I_{PP}, V_{EE}	= 2.5 V	= 4.5 x $10^{-9}\dot{\gamma}\mu A$

3.3.2 SMALL GEOMETRY Q2, Q3

Parameter		
BV_{CBO}, I_C	= 100 μA	>25 V
BV_{CEO}, I_C	= 5 mA	<7 V
BV_{EBO}, I_C	= 100 μA	>6.5 V
H_{FE}, I_C	= 140 A at -55° C, post-neutron	>7
$V_{CE(SAT)}$, I_C	= 300 μA at 125° C β_F = 4	<0.3 V
V_{BE}, I_B	= 2 μA at 125° C	>500 mV
V_{BE}, I_B	= 50 μA at 125° C	<620 mV
V_{BE}, I_B	= 150 μA at -55° C	<950 mV
C_{OB}, V_{CB}	= 2.5 V	<0.3 pF
C_{IB}, V_{EB}	= 0.5 V	>0.4 pF
I_{PP}, V_{CB}	= 4 V	= 2.8 x $10^{-8}\dot{\gamma}\mu A$

3.3.3 OUTPUT GEOMETRY Q4, Q5

Parameter		
BV_{CBO}, 100 μA		>25 V
BV_{CEO}, 5 mA		>7 V
BV_{ECO}, 100 μA		>6.5 V
H_{FE}, I_C	= 1.3 mA at -55° C post-neutron	>13
$V_{CE(SAT)}$, I_C	= 2 mA at 125° C pre-neutron β_F = 10	<0.3 V
$V_{CE(SAT)}$, I_C	= 1.3 mA at 125° C post-neutron β_F = 11	<0.3 V

V_{BE}, I_B	= 6 μA, +125° C	>530 mV
V_{BE}, I_B	= 300 μA -55° C	<1000 mV
I_{CBO}, V_{CB}	= 2.4 V at 125° C	<10 A
C_{OB}, V_{CB}	= 2.5 V	<0.85 pF
C_{IB}, V_{BE}	= 0.5 V	<0.6 pF
I_{pp}, V_{CB}	= 2.5 V	= 3.5 x 10^{-8} $\dot{\gamma}\mu$A

3.4 THIN FILM RESISTORS

Following are the layout ground rules used for the thin film resistors:

- Resistor width (minimum) = 0.5 mil
- Resistor separation (minimum) = 0.5 mil
- Aluminum-resistor overlap = 0.5 mil; on sides 0.2 mil
- Resistor to aluminum = 0.4 mil
- Resistor to diffusion = 0.4 mil

3.5 ALUMINUM INTERCONNECT

The following were minimum layout ground rules for metal interconnect:

- Metal width = 0.4 mil
- Metal separation = 0.4 mil
- Metal aperture overlap = 0.1 mil

SECTION IV

MANUFACTURING PROCESSES

4.0 GENERAL

Because the principal objective of the program was to advance the processes and techniques used to produce chrome silicon thin film resistors, this section will be devoted to summarizing the approaches considered, the equipment used, and the process refinements deemed necessary as a result of the thin film efforts.

4.1 THIN FILM PROCESS

Reference is made to Paragraph 2.1.1 to define the objectives required for the thin film resistors to be used in the integrated circuit logic.

On the basis of earlier studies by Harris' Advanced Process Development Section, the metal material chosen was a silicon chromium mixture since it offered the desired range of electrical properties and metallurgical compatibility with aluminum and silicon dioxide. Investigation was done with sputtering cathodes having four different compositions.

Deposition modes studies were sputtering and thermal evaporation. It was determined that no technique of thermal evaporation, including electron beam, provided a stoichiometric or even a reproducible process when multielement materials are evaporated. Sputtering, however, was established to be a stoichiometric process and also had the advantages of greater film adhesion and purity. Sputtering parameters that affected certain major film properties were also studied. The following sputtering parameters were selected for pilot production of the demonstration vehicles under the contract:

- Cathode potential
- Argon pressure
- Background pressure
- Source spacing

The following major film characteristics were considered:

- Resistivity
- Temperature coefficient of resistivity

- Stability
- Resistivity range
- Voltage coefficient of resistivity (resistor linearity)

All the items listed here will be elaborated on in succeeding portions of this section of the report.

Initially, the sputtering system itself will be discussed. Next, the sputtering parameters will be elaborated on, followed by a discussion of the material characterization.

4.1.1 SPUTTERING EQUIPMENT

The sputtering system is instrumented to precisely measure and, where possible, automatically control the critical deposition parameters: argon pressure, cathode voltage, background pressure, and deposition time. Cathode-substrate spacing is optimized for film thickness uniformity and is a fixed parameter. The complete system configuration is shown in Figure 11.

4.1.1.1 Deposition Chamber

The chamber contains a single 5-inch diameter cathode mounted above a rotating wafer carrier that has a 10-slice capacity. Shields and a shutter are configured to allow pre-sputtering and to prevent oblique angle deposition. A Meissner trap is mounted in the chamber to aid in removal of reactive gasses during the pump down and deposition cycles.

4.1.1.2 Pumping System

Vacuum pumping is accomplished using a 2400 lps diffusion pump backed by a 17.7 cfm mechanical pump. A liquid nitrogen trap is located between the diffusion pump and high vacuum value. An ionization gauge is mounted in the deposition chamber for high vacuum measurement. During sputtering, the high vacuum value is throttled to achieve a predetermined argon flow rate.

4.1.1.3 RF Power System

The RF generator is capable of delivering 1 kW at 13.56 mc. The generator output is coupled to the cathode through a matching network located directly above the cathode. A Harris designed automatic power control circuit has been incorporated which maintains a constant preset power level at the cathode in the event of load fluctuations or drift in the generator.

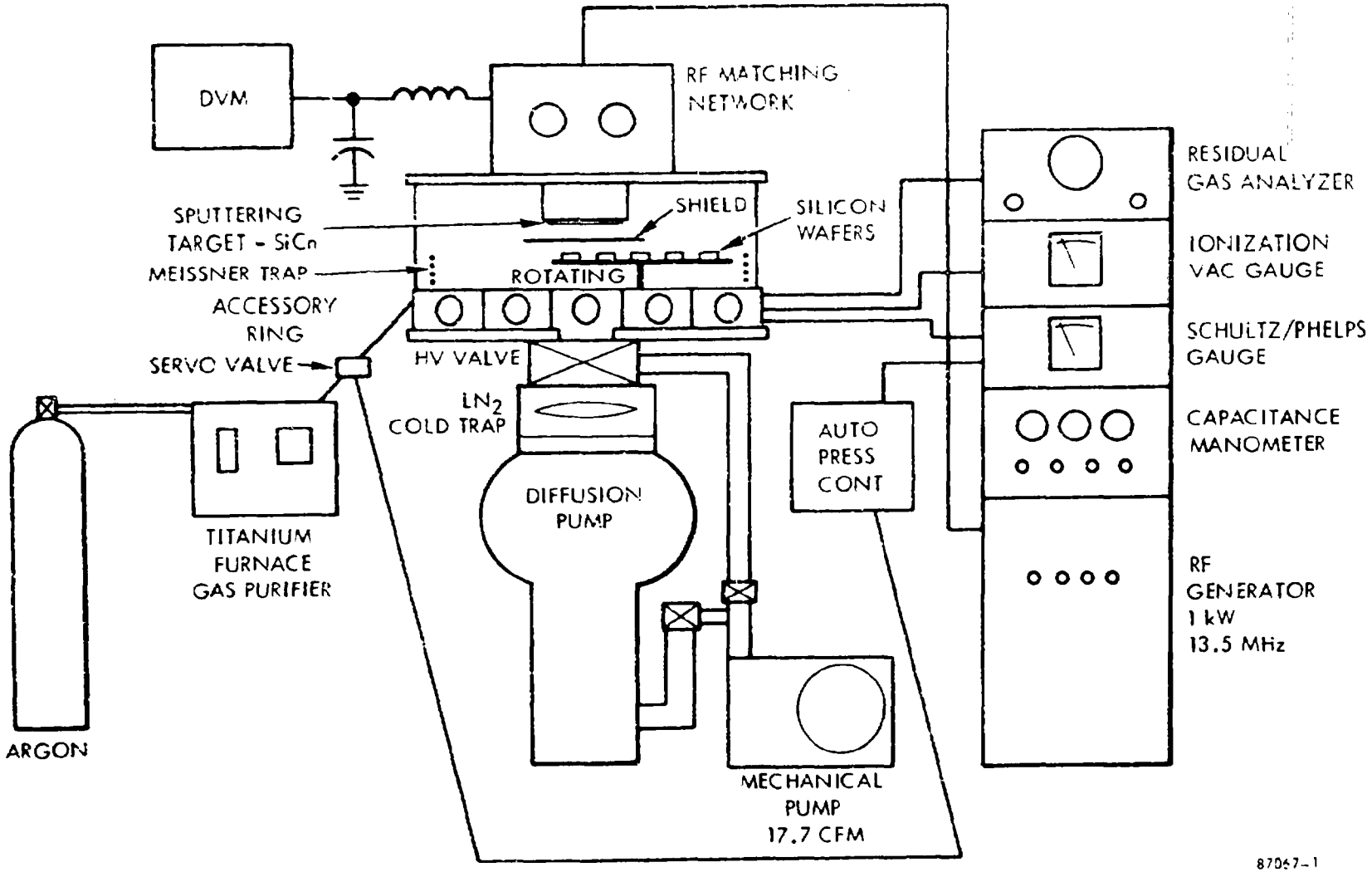


Figure 11. RF Sputtering System

4.1.1.4 Argon System

High purity argon is further refined by a titanium furnace prior to introduction into the sputtering chamber. Argon pressure is sensed by a high pressure Shultz Phelps ionization gauge that is close looped to an automatic pressure controller and servo valve. Pressure measurement accuracy is ensured by the use of a capacitance nanometer as a calibration reference.

4.1.2 SUMMARY OF SPUTTERING PARAMETER STUDIES

4.1.2.1 Cathode Potential

Rate of deposition and film bulk resistivity were found to be more dependent on cathode potential than on any of the other parameters regardless of cathode composition. Rate of deposition was identical for all compositions and is depicted in Figure 12. Cathode potential also has a pronounced effect on bulk resistivity as shown in Figure 13. Increasing the potential from 1 kV to 2 kV results in a 50 percent decrease in bulk resistivity for all of the compositions studied. It is assumed that this phenomenon is caused by increasing film density resulting from higher cathode potentials.

4.1.2.2 Argon Pressure

During sputtering, the number of argon ions available to bombard the cathode influences the rate of deposition. However, in our studies, a saturation condition occurred at an argon pressure of 9 microns. Further increase in pressure did not significantly increase deposition rate. Figure 14 depicts rate as a function of pressure at cathode potentials of 1.0, 1.5, and 2.0 kV. Film bulk resistivity was found to be independent of pressure.

4.1.2.3 Background Pressure

Background pressure is defined as that pressure attained at the completion of the pump down cycle and prior to admitting argon into the sputtering chamber.

To characterize this parameter, a series of depositions were performed at background pressures ranging from 5×10^{-5} to 2×10^{-8} Torr. Film resistivity control became erratic at pressures above 5×10^{-6}. At lower pressures, run to run resistivity repeatability exhibited no dependence on pressure.

4.1.2.4 Cathode - Substrate Spacing

This parameter was studied to determine its influence on film thickness uniformity across a 2-inch diameter silicon wafer. Spacings from 3 to 8 cm were evaluated and it was found that the best uniformity, ±2.5% was attained at approximately 8 cm.

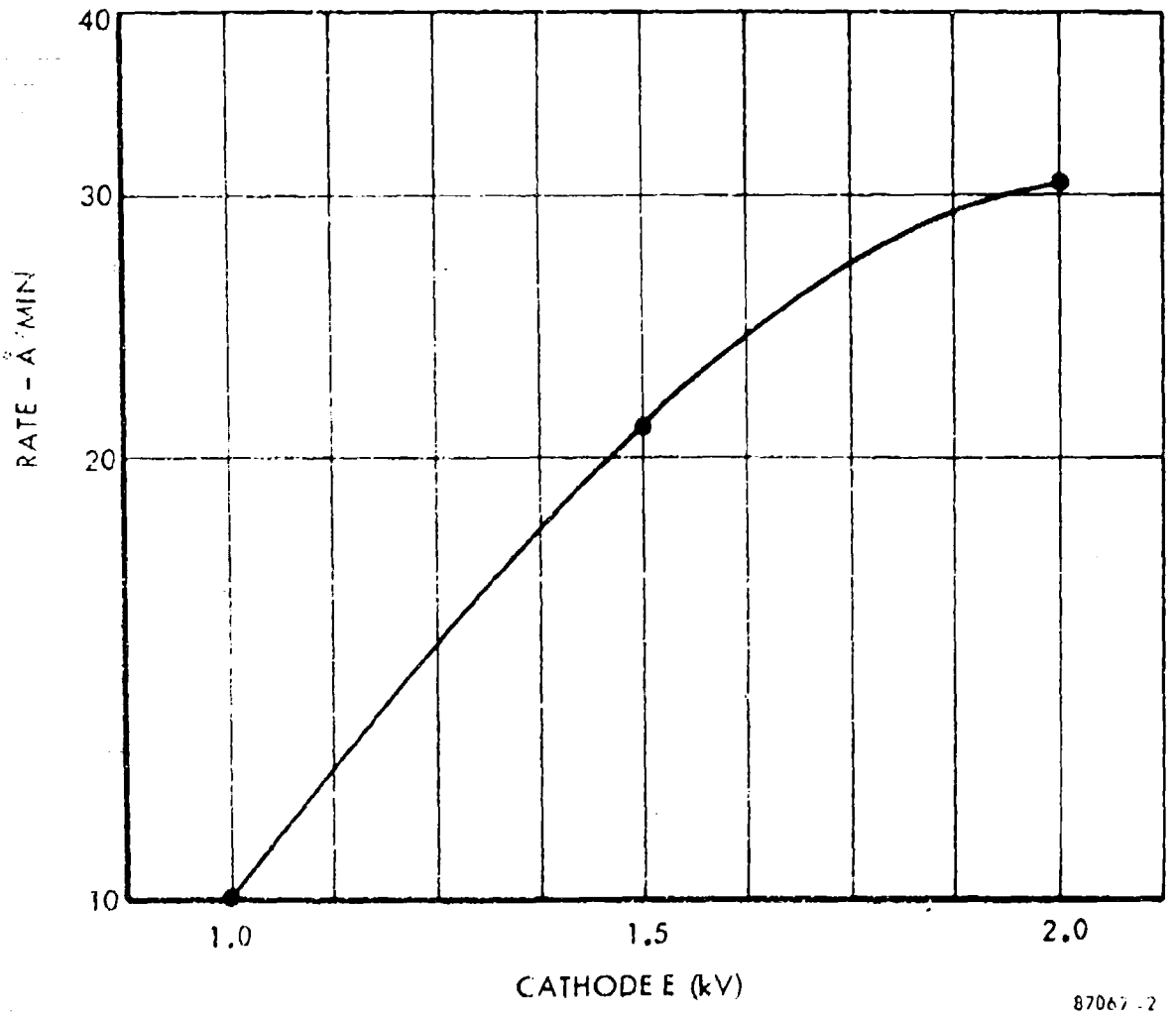


Figure 12. Rate versus Cathode Voltage (23% Cr-RF Sputtered)

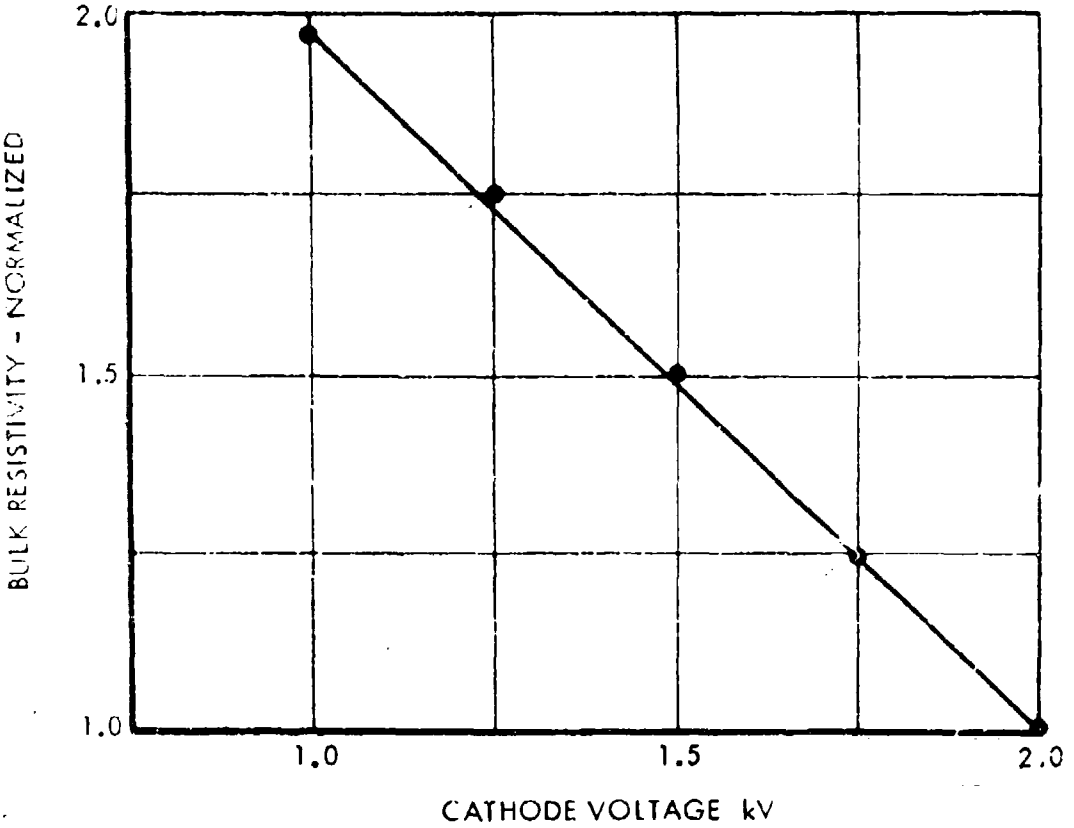


Figure 13. Resistivity versus Cathode Voltage (RF Sputtered CrSi)

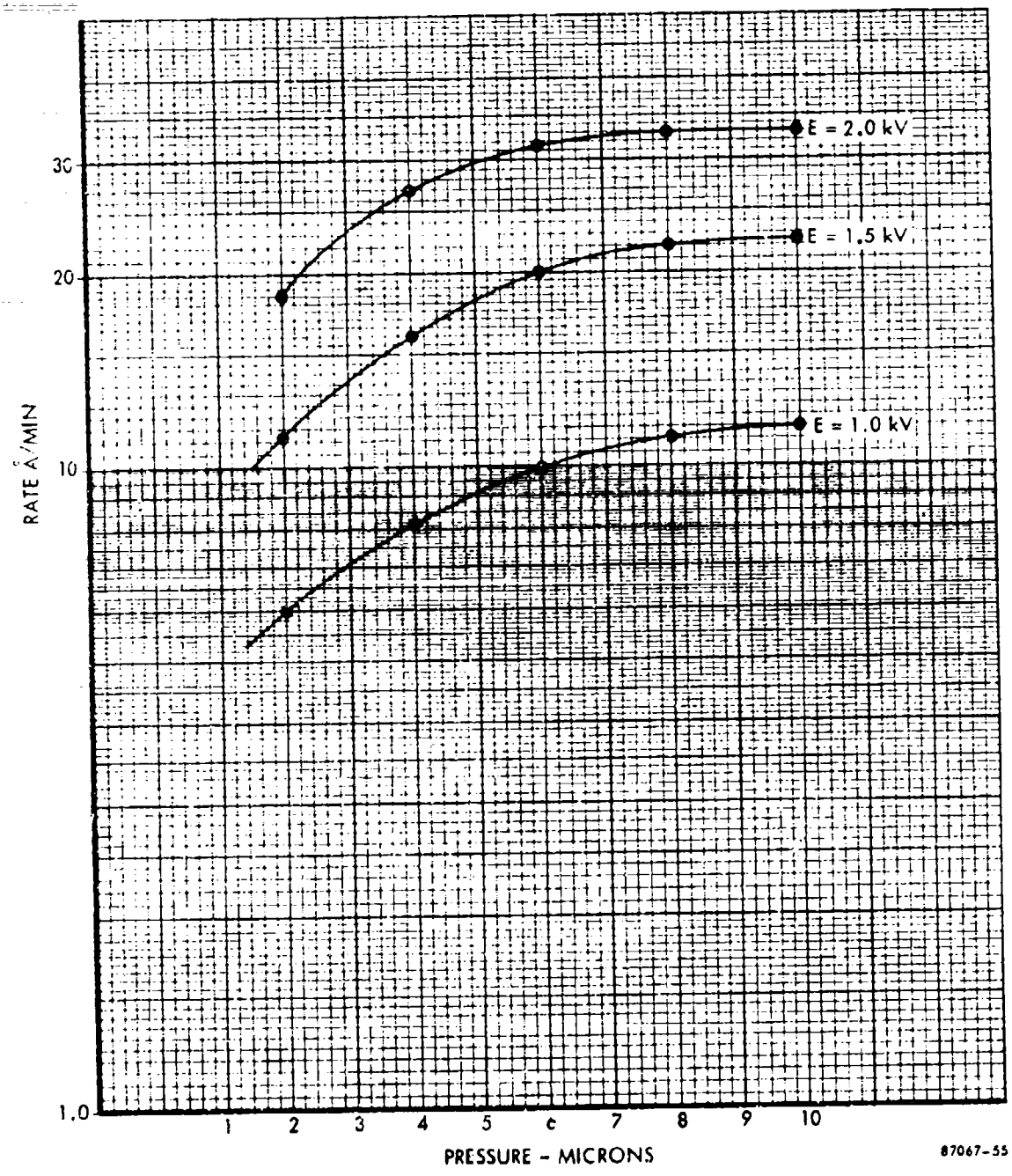


Figure 14. Rate of Deposition versus Argon Pressure (28% CrSi)

4.1.2.5 Deployed Deposition Parameters

Based on the studies, the following deposition parameters were selected for all subsequent material studies and for processing the Wright-Patterson devices.

Cathode - substrate spacing	6 cm
Cathode potential	1.0 kV
Argon pressure	10 microns
Background pressure	5×10^{-7} Torr

4.1.3 MATERIAL CHARACTERIZATION

4.1.3.1 Cathode Composition

Four cathode compositions were studied:

Composition No.	Chromium (At. %)	Silicon (At. %)
1	33	67
2	28	72
3	23	77
4	18	82

A series of 5 depositions were done with each composition to a target thickness of 200 angstroms. Substrates were oxidized silicon wafers. Films were delineated chemically using a test pattern containing linewidths from 0.25 to 2.0 mils. Contacts were thermally evaporated aluminum, also chemically delineated. Resistors were then stabilized by annealing at approximately 500° C in a nitrogen atmosphere.

4.1.3.2 Resistivity

Resistors were then probed and resulted values plotted in terms of sheet resistivity (Figure 15). It is seen that nearly a decade of resistivity values was obtained with Composition No. 1 at 700 ohms/square and Composition No. 3 yielding 6000 ohms/square.

4.1.3.3 Temperature Coefficient of Resistivity (TCR)

Temperature coefficient of resistivity (TCR) measurements were performed on samples from all compositions. Individual devices were assembled in TO84 packages and resistance measurements taken at temperatures from 50° C to 150° C in 25° C increments. Resultant TCR data is shown in Figure 16. Again, a range of values was obtained depending on composition: +400 ppm/° C for

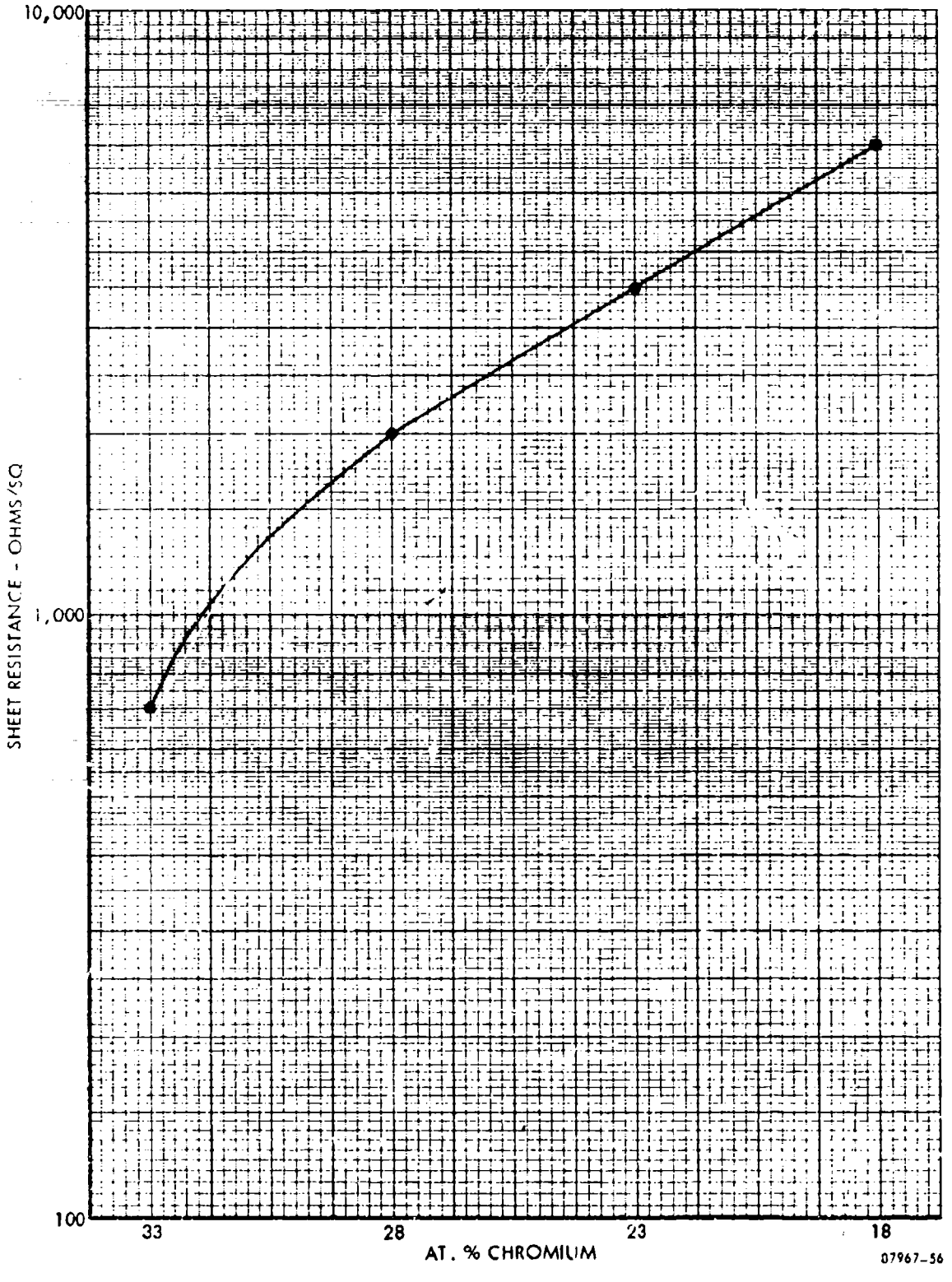
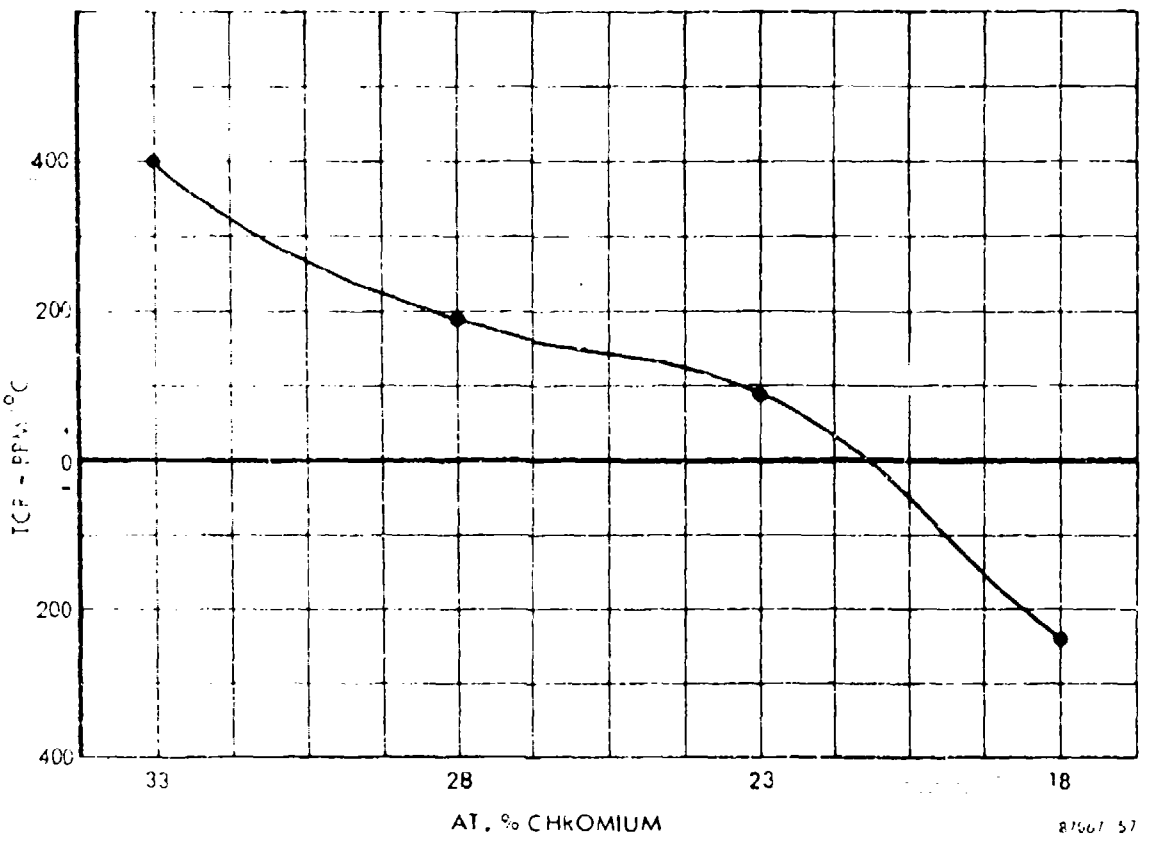


Figure 15. Sheet Resistance versus Percent Chromium Thickness



RF Sputtered CrSi @ 1 kV

Figure 16. Temperature Coefficient of Resistivity versus Percent Chromium

Composition No. 1 and -240 ppm/^{o} C for Composition No. 4. TCR's were linear over the stated temperature range for all compositions.

4.1.3.4 Stability

Initial stability data was obtained by packaging 5 resistors from 5 runs of each of the compositions and conducting load life stress testing. The resistors were 1 x 8 mils, and were stressed at 100 mW and 150^{o} C for 1000 hours.

Results of the test demonstrate that all compositions are stable. Worst-case resistance drift occurred on Composition No. 4 samples where one run (5 units) exhibited a ΔR of 3 percent. Composition No. 3 samples had ΔR drift of less than 2 percent and Compositions No. 2 and No. 1 samples exhibited ΔR's of less than 1.5 percent.

4.1.3.5 Resistivity Range

Run to run short resistivity spread for the 5 depositions performed with each of the compositions is shown in the following table.

Composition	Resistivity Range (%)
1	±5
2	±7
3	±10
4	±15

The range (%) is around the average values of sheet resistivity for the four compositions as shown in Figure 15.

4.1.3.6 Voltage Coefficient of Resistivity (Resistor Linearity)

Resistors fabricated from all compositions were tested for I-V characteristics using a curve tracer. Typical traces are shown in Figure 17. It can be seen that I-V relationships are linear except at very high power levels.

4.1.4 FABRICATION PROCESS

4.1.4.1 Process Target Parameters

Circuit design and layout considerations for the devices to be fabricated dictated a thin film resistor sheet resistivity of 1500 ohms/square would be optimum. Based on the material characterization of the four chrome silicon compositions, Composition No. 2 (28 percent Cr - 72 percent Si) was selected for use on these circuits. The temperature coefficient of resistivity for

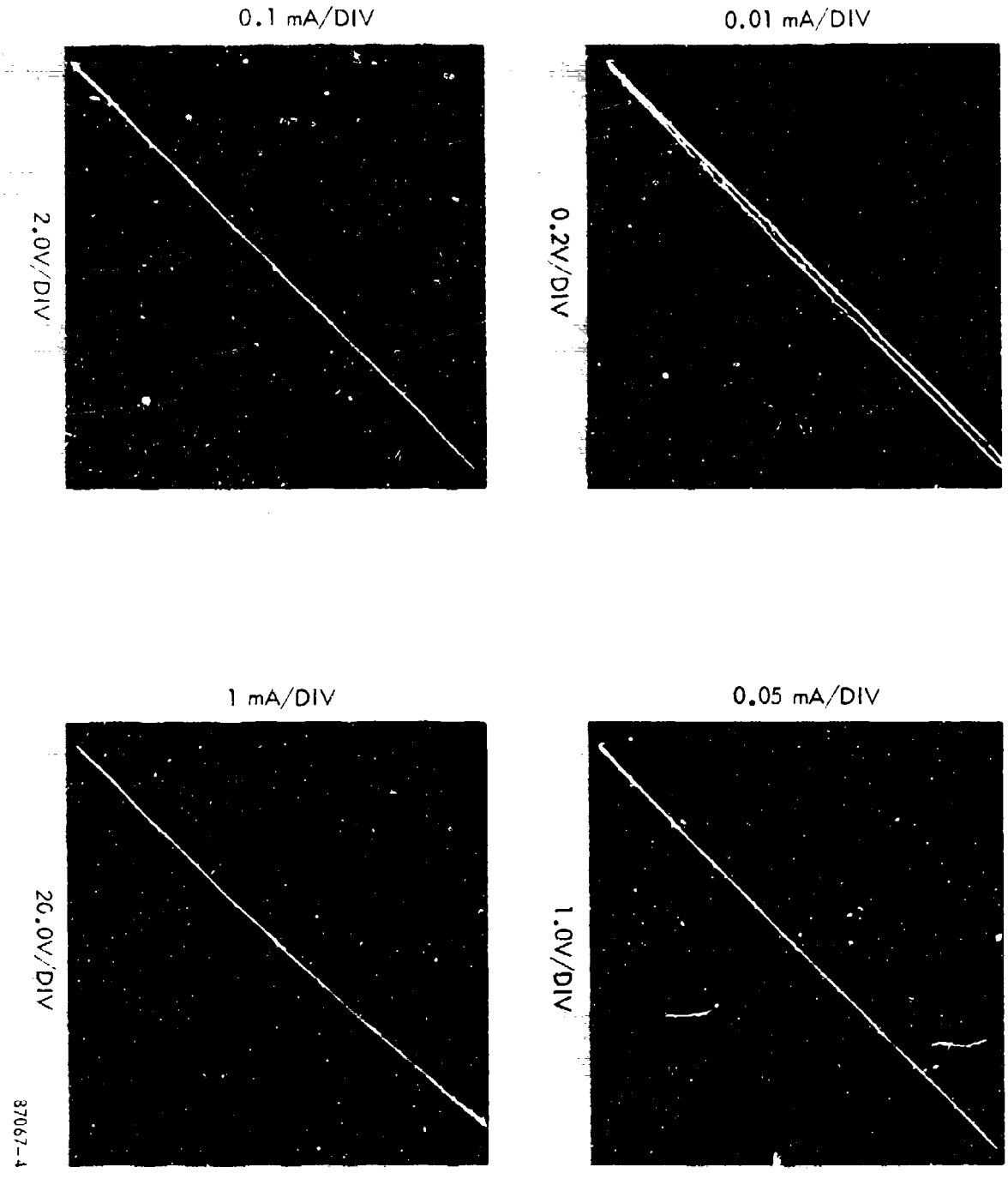


Figure 17. Curve Tracer Characteristics (6000 ohms/sq. Resistor)

this combination is approximately +180 ppm/^{o} C. Using this process techniques combined with the layout ground rules of Paragraph 3.4, the maximum resistor variation from nominal value was less than 20 percent.

4.1.4.2 Sputtering Procedure

The following procedure was adapted for the sputtering of the thin film chrome silicon resistors for this program.

- Load wafers into chamber and evacuate to 5 x 10^{-7} Torr.
- Admit argon to 10μ and with shutter closed, pre-sputter cathode at 1.0 kV.
- Commence wafer carrier rotation, open shutter and sputter for approximately 30 minutes.
- Close main valve and lock fill system with nitrogen. Remove wafers.

4.1.4.3 Etch Process

Delineation of the resistors and compatibilities with aluminum and silicon dioxide were investigated by means of a test mask which contained resistors as narrow as 0.25 mil. Both reverse and direct etch were studied. It was determined that direct etch, using a negative photoresist and an acid etch solution, provided optimum definition. Microphotographs of two magnifications of the resistor test pattern are shown in Figure 18, which reveals an excellent definition of the 0.25 mil resistor. No contact resistance problem between the aluminum interconnect and the chrome-silicon resistors was detected during test mask evaluation. The silicon dioxide receiving the resistors caused no detectable structural anomalies.

4.1.4.4 Process Flow

The process flow developed by Harris Semiconductor for the fabrication of chrome-silicon metal film resistors is listed below. The process flow begins after all diffusion steps have been completed.

Step	Description
1	Pre-evaporation clean
2	Slice drying
3	Chrome-Silicon deposition - AC sputtering Resistivity = 1500 ohms/square Source material = 28% Chrome

Step	Description
4	Photoresist coat - KMER
5	Photoresist bake - 30 minutes @ 100° C
6	Photoresist exposure - resistor mask
7	Photoresist develop - conventional
8	Pre-etch bake - vacuum - 150° C
9	Etch - HCl
10	Solvent clean - organic
11	Slice drying
12	Photoresist coat (for oxide aperture etch) - KMER
13	Photoresist bake - 30 minutes @ 100° C
14	Photoresist exposure - all aperture mask
15	Photoresist develop - conventional
16	Pre-etch bake - vacuum - 150° C
17	Etch - HF
18	Solvent clean - organic
19	Slice drying
20	Aluminum evaporation - 40 microinches
21	Photoresist coat - KMER
22	Photoresist bake - 30 minutes @ 100° C
23	Photoresist exposure - interconnect mask
24	Photoresist develop - conventional
25	Pre-etch bake - vacuum - 150° C
26	Etch - HNO_3
27	Resistor stabilization bake - 30 minutes @ 500° C
28	Ultrasonic clean

Step	Description
29	SiO_2 deposition - 10,000 Å
30	Photoresist coat - KMER
31	Photoresist bake - 30 minutes @ 100° C
32	Photoresist exposure - SiO_2 mask
33	Photoresist develop - conventional
34	Pre-etch bake - vacuum - 150° C
35	Etch - HF
36	Solvent clean - organic

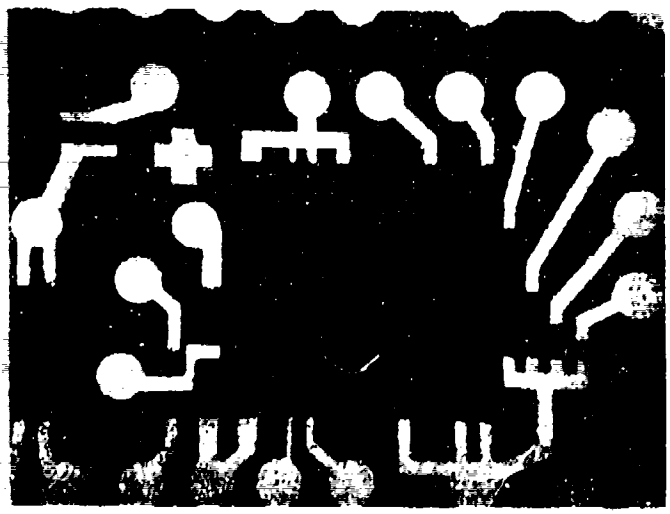
4.1.5 PROCESS IMPROVEMENTS

The internal development program resulted in a process which was basically sound, requiring no changes in the overall approach to fabricating chrome-silicon resistors. However, the fabrication of resistors during the internal development program was carried out in small lots by engineers and skilled technicians. It was the objective of this contract to identify those areas of the chrome-silicon resistor fabrication process that were not readily adaptable to high volume production, to propose and implement the necessary process changes that achieve producibility, and to illustrate the effectiveness of these changes by processing a significant number of integrated circuits employing chrome-silicon resistors in a manufacturing environment.

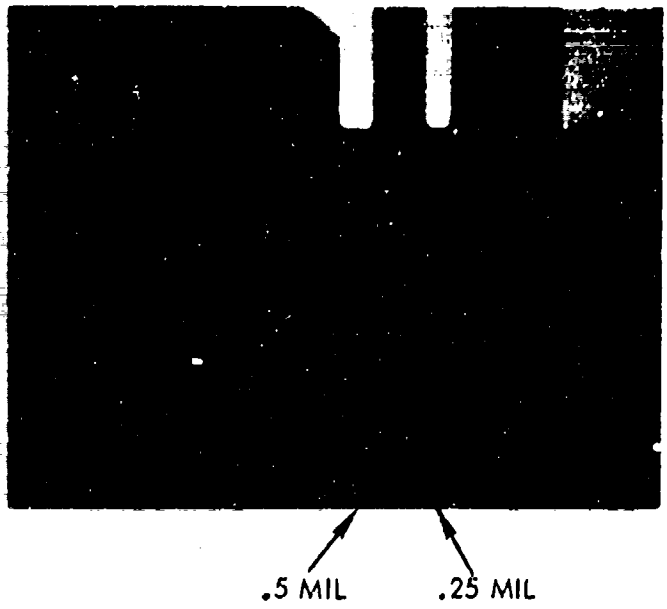
The following is a discussion of those steps identified as critical to the process. In order to improve their suitability to the manufacturing environment, process changes are discussed for certain steps.

4.1.5.1 Pre-Evaporation Clean

No changes in the normal cleaning process are thought to be required. Usually, metal film is affected by the cleanliness of the surface. Since chemicals on the surface may react with the metal being deposited, either during deposition or during subsequent high temperature steps, the structure and, therefore, the resistivity of the metal film may change. However, chrome-silicon is relatively insensitive to these effects for a number of reasons. First, the resistor film is thick enough that structural changes in the metal layer in contact with the silicon dioxide surface have little effect. Second, sputtering, in effect, cleans the surface. No critical sensitivity to the pre-evaporation clean was noted during the internal development program. The resistors fabricated during development were deposited on silicon pilot



44 X MAGNIFICATION



180 X MAGNIFICATION

87067-5

Figure 18. CrSi Resistor Test Pattern

slices on which various oxides have been grown, including both undoped and phosphorus doped silicon dioxide, and silicon nitride. Thus, the surface conditions were similar to what would be found on slices which have been through the complete integrated circuit fabrication process.

4.1.5.2 Chrome-Silicon Deposition

This is the most critical step in the process. The three most critical parameters influencing the metal film during sputtering are background pressure, argon pressure, and cathode current density (or voltage). These parameters all affect the deposition rate of the chrome-silicon. Since the plasma makes monitoring of actual resistivity during sputtering impossible, the correct resistivity depends on controlling time of deposition and deposition rate. In order to control the accuracy at which the deposition rate is known, it was imperative that the three critical parameters be controlled. First, control of background pressure during the sputtering is limited to the particular sputtering system being used. Effective control is based on making certain that the operator waits until an acceptable vacuum has been achieved before allowing the sputtering operation to begin. Although automatic control would be desirable, consideration of this problem was not necessary for the manufacturing environment.

During the internal development program, argon pressure was monitored using a Pirini gauge and was manually controlled by an operator. The Pirini gauge bases pressure measurements on the thermal conductivity of the gas. The gauge is influenced by the temperature of the room and may drift ±1 - 2 microns during a single sputtering run and ±3 - 5 microns over long periods. In addition, there are the inherent inaccuracies in manual control such as operator reading error, and diligence in maintaining the set point by repeated adjustment. Figure 14 discloses that even a perfect operator cannot achieve more than ±5% resistivity control due to the ± micron drift of the Pirini gauge.

Since the accuracy and reproducibility of the system described was undesirable, it was recommended that the Pirini gauge be replaced with a capacitance manometer. This manometer would provide accuracy of ±0.1 micron traceable to the Bureau of Standards. Furthermore, an automatic closed-loop control system was installed which will sense the diaphragm deflection of the manometer and act to maintain the desired set point.

Finally, during the internal development program, the cathode current density was controlled manually by the operator who monitored the current density by measuring cathode voltage with a galvanometric voltmeter, accurate to ±5%. Figure 12 shows that this voltmeter inaccuracy alone causes a ±8% variation in sputtering rate. The galvanometric voltmeter has been replaced with a digital voltmeter, accurate to ±0.05%. Furthermore,

consideration was given to the design and construction of a closed loop control system that uses the digital voltmeter monitor to maintain the set point.

4.1.5.3 Resistor Stabilization Bake

The study further indicated how the resistors were affected by processing subsequent to the deposition including a.l exposure to chemical agents and temperature cycles. It was determined that a high temperature stabilization bake for the resistors was necessary in order to stabilize the resistivity so that no shifts would occur at temperatures encountered during contact baking, die attach, and package sealing. A graph showing the typical effects of stabilization baking on resistor value is shown in Figure 19. The flatness of the curve demonstrates the stability of the resistivity to ambient temperature and the absence of interaction with the aluminum interconnect.

The resistor stabilization bake is intended to eliminate changes in resistor values during subsequent processing. These changes occur due to thermally induced structural changes such as oxidation. It has been found that baking the resistors at 500° C, a temperature substantially above those reached during subsequent processing, renders resistor values stable. As can be noted from Figure 19, the temperature control during the 500° C bake is not critical. No changes in this stabilization bake were necessary during the contract.

4.1.5.4 Aluminum Evaporation Process Step

This step is potentially critical due to the requirement of sufficiently cleaning the contact apertures prior to aluminum deposition in order to assure a successful evaporation without adversely affecting the thin film resistors. If cleaning is not sufficient, poor or no electrical contact between the semiconductor devices and the aluminum becomes a critical problem. Note, that even though poor contacts can sometimes be improved during subsequent high temperature cycling, this will cause an unpredictable resistance change which leads to inaccurate resistor values. It has been determined that an acid clean is necessary prior to the aluminum evaporation and that this clean will attack the chrome-silicon resistors, reducing their thickness and raising their resistance values. Therefore, it was necessary that the parameters of the cleaning operation be closely controlled to render the resistance change predictable. The degree of control required was within the capabilities of a manufacturing environment. Previously, such control of cleaning steps was not required; therefore, it was necessary to indoctrinate the manufacturing personnel in the control of the cleaning process.

The interconnect aluminum was evaporated to a thickness of one micron (40 - 50 microinches) with a sheet resistivity of 0.028 ohm per square. This ensured that the aluminum deposited

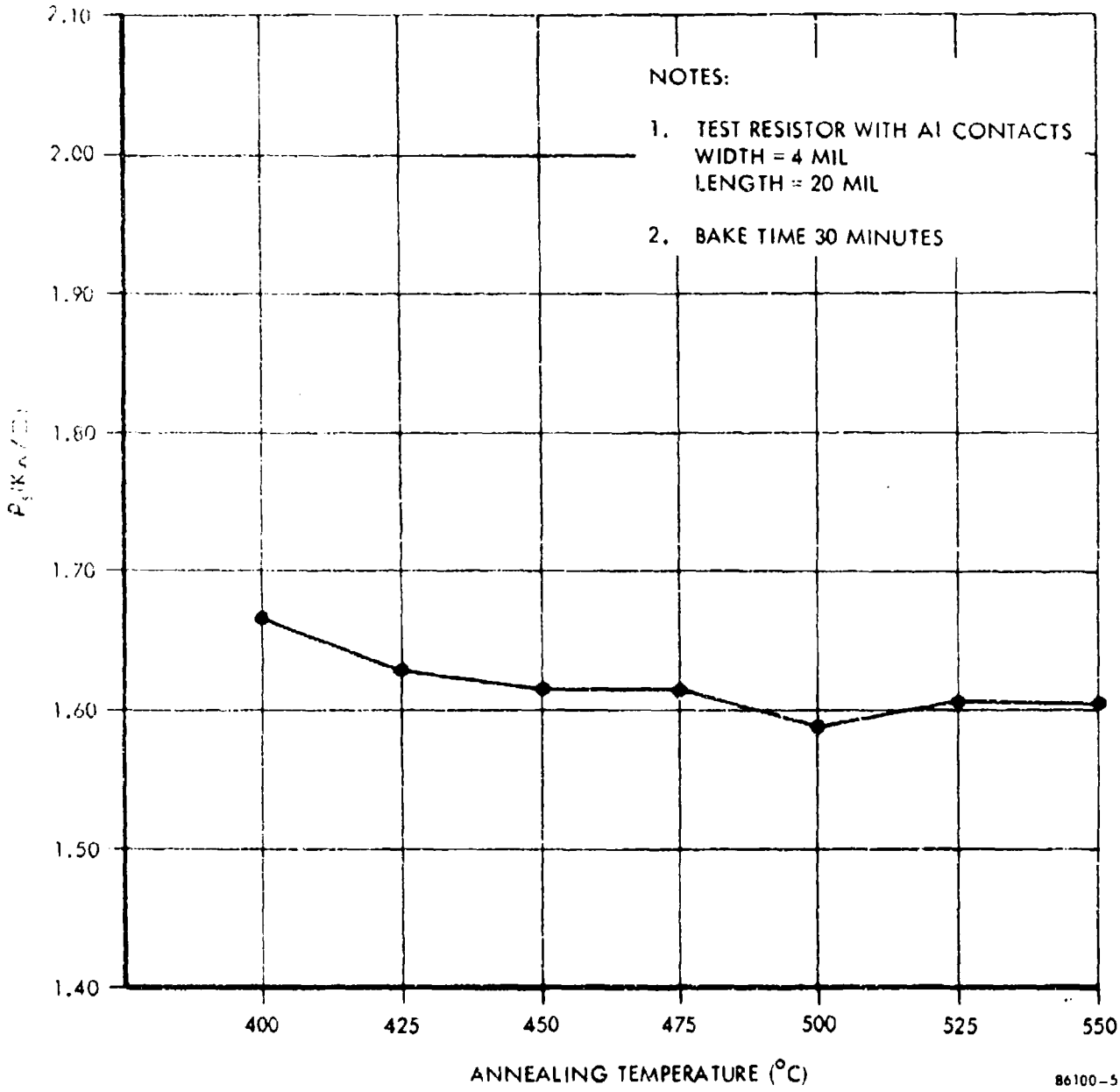


Figure 19. Stabilization Baking of a CrSi Resistor

on a forty-five degree oxide step would have a thickness of at least 0.7 micron. The metal width was varied for different sections of the circuits to ensure that the interconnect would not be damaged during any instances of shorted junctions during gamma irradiation.

SECTION V

RESULTS

5.0 GENERAL

Included in this section are the results found in the major areas of wafer fabrication, chip layout, and electrical performance.

5.1 RUN HISTORY

A total of 9 wafer runs was required on Phase I and Phase II to achieve the total delivery requirement of 600 pieces each of the two device types. Although the throughput yields were lower than predicted, it was concluded that the improvements of Phase II production were significant enough to allow the following two conclusions to be formulated:

- An acceptable repeatable manufacturing process for the fabrication of chrome-silicon resistors has been achieved.
- Sufficient knowledge and skill have been attained with the manufacturing process to allow more accurate predictions of yields on future production runs.

5.2 FABRICATION PROBLEMS

Fabrication problems associated with Phase I included both device layout and process problems. The process problems were elaborated on in Section 4.0.

5.2.1 DEVICE LAYOUT LIMITATION

As will be discussed in detail in Paragraph 5.4.2.2, an increase in propagation delay on the gate with the extender was experienced with the Dual Four Input Gate due to extra capacitance associated with the extender node. To compensate for this, a change was made in the N+ emitter mask to reduce the skew in the propagation delay. The modification eliminated the N+ crossunder channel. Only minor improvement resulted from this change. Based on the results obtained following this mask change, along with a theoretical analysis of the electrical model, it was concluded that the effect was due to the added capacitance contributed by the bond pads used for the extender, along with the package capacitance for these pads. An analytical analysis of the problem will be presented in Paragraph 5.4.2.2.

5.3 CHIP LAYOUT

After completion of the final device layouts, it was decided to make a comparison between a compatible 54H series hardened circuit processed with 200 ohms per square nichrome resistors and the 54L circuits utilizing 1500 ohms per square chrome-silicon resistors as developed on this program. The comparison was made for both the Dual D Flip-Flop and the Dual Four Nand Gate. The purpose of the comparison was to illustrate the chip area reduction resulting from the use of the high resistivity thin film resistors.

5.3.1 DUAL D FLIP-FLOP (54L/H74)

	54L74	54H74
Active device area	272 mil^2	1112 mil^2
Resistor area	401 mil^2	836 mil^2
Resistor values	289 kΩ	27 kΩ
Chip area	68 x 51 3468 mil^2	73 x 80 5840 mil^2
Border area	1352 mil^2	2100 mil^2
Border including bond pads as a percentage of total chip area	39%	36%

Although the 54L74 has an order of magnitude more resistant than the 54H74, the chip, as a result of adding high resistivity thin film resistors, is only sixty percent the size of the 54H74. A drawing of the 54L74 interconnect is shown in Figure 20.

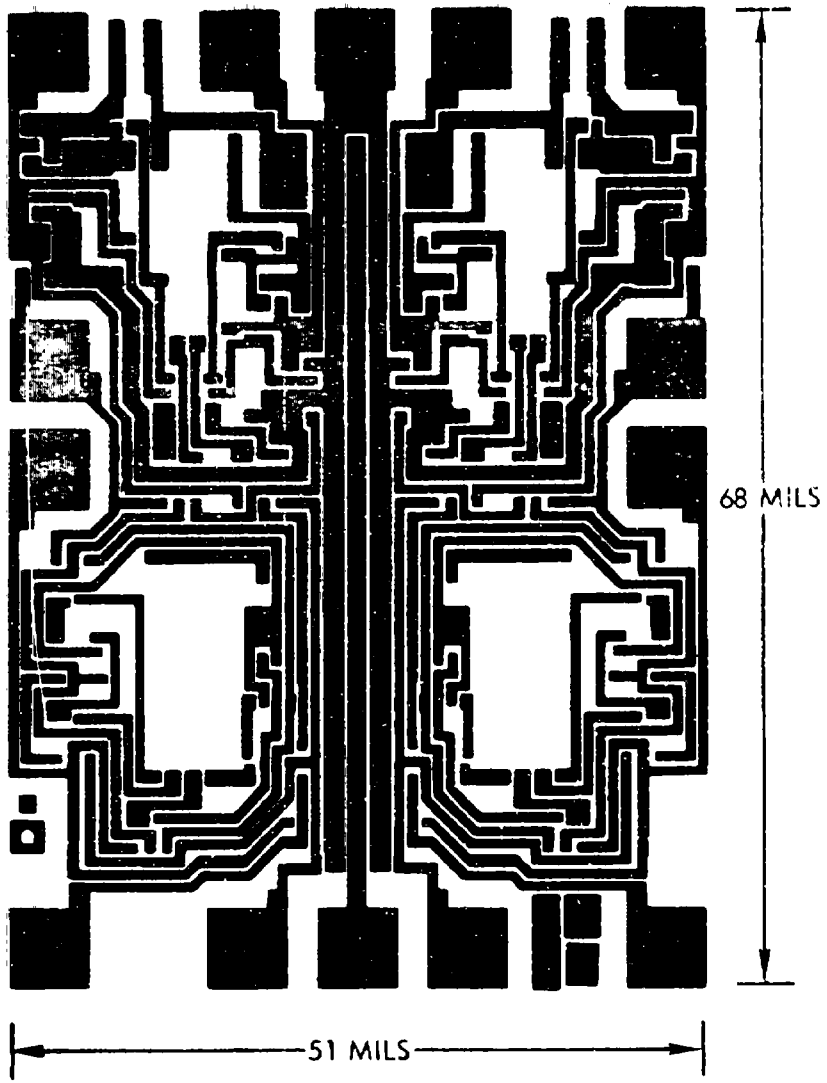
If the nichrome resistors had been used for the 54L74, the chip area required can be estimated as 8850 mil^2 or 2.5 times the chip area required using chrome-silicon resistors.

5.3.2 DUAL FOUR NAND GATE (54L/H20)

Similar comparisons can be made with the Dual Four Nand Gate. The 54L20 is 63 percent the size of the 54H20.

	54L20	54H20
Chip size	47 x 42	56 x 56
Chip area	1975 mil^2	3140 mil^2

A drawing of the 54L20 interconnect is included in Figure 21.



DUAL D FLIP-FLOP
54L74

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Figure 20. Interconnect Pattern (Flip-Flop)

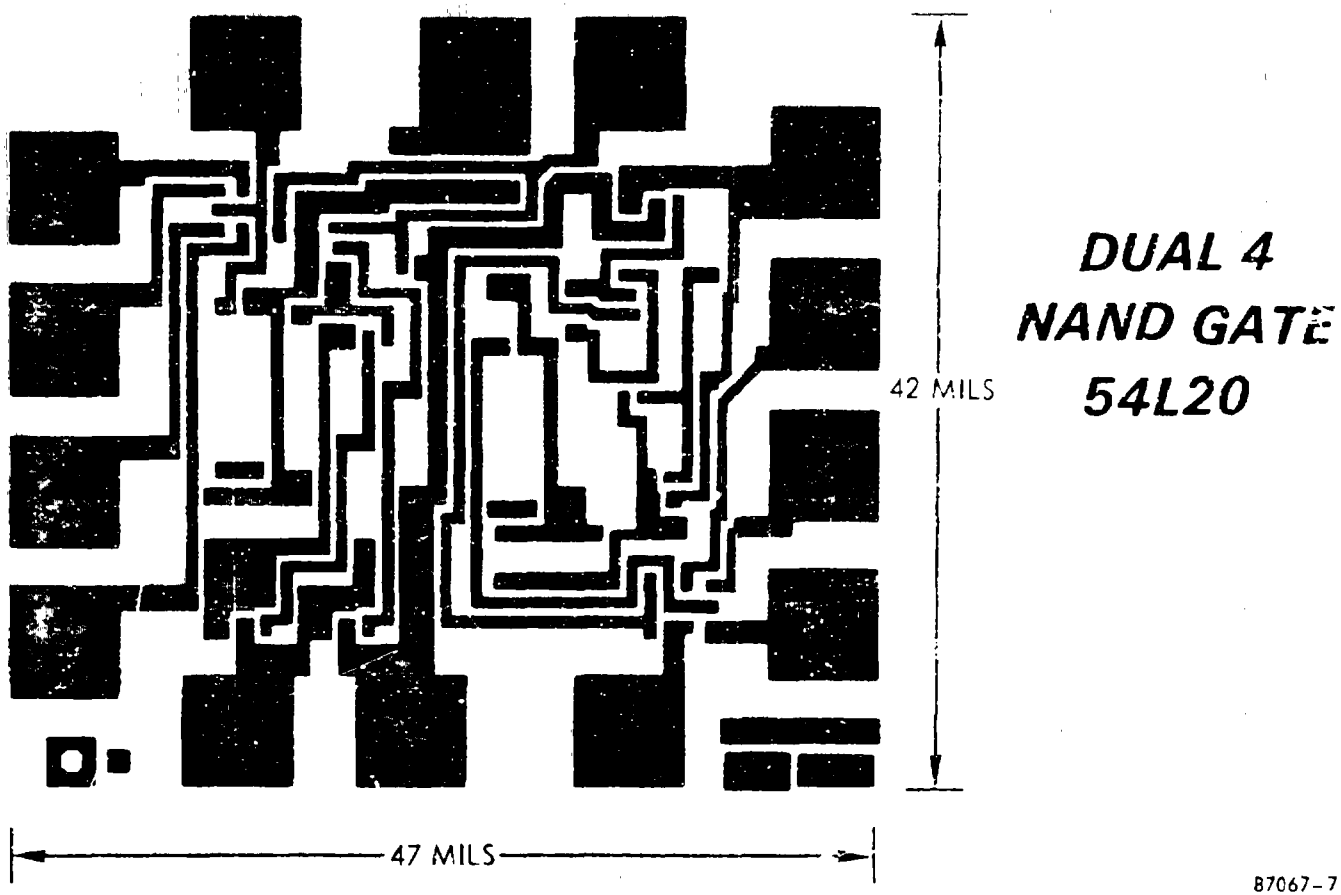


Figure 21. Interconnect Pattern (Dual 4 Gate)

5.4 ELECTRICAL PERFORMANCE

5.4.1 PARAMETRIC TESTS

Data compiled on completed devices indicated the design goals on parametric limits as defined in Paragraph 2.2.2 were attained.

To obtain the parametric data for each type device, it was necessary to develop and compile a DC test program capable of evaluating the performance of the device. Tables V and VI define the parametric test conditions used to evaluate the Dual D Flip-Flop and Dual Four Nand Gate, respectively.

5.4.2 PROPAGATION DELAY MEASUREMENTS

5.4.2.1 Dual D Flip-Flop

For all practical purposes, the switching speed predictions of the flip-flop were attained. The propagation delays were somewhat slower than predicted but this was attributed to the interconnect complexity and density, which attributed more capacity per unit area than originally predicted in the calculations. However, it was concluded that the flip-flop switching speeds did meet the objectives set originally.

5.4.2.2 Dual Four Nand Gate

The propagation delays of the dual gate were also found to meet and exceed the design goals for switching speed. It was found that the gate with the extender exhibited propagation delays of approximately 25 ns greater than the gate with no extender.

It is logical why the gate with the extender is slower as offered by the following explanation. However, the gate did empirically exhibit more delay than the analytical calculations predicted.

The reason the propagation delays differ is because there is added capacitance on the collector of the input transistor caused by the addition of the extender. In order to avoid flying leads (interconnect outside the bonding area), it is necessary for one of the extender leads to cross under the V_{CC} line. This cross under and the bond pads of the extenders add capacitance to the collector of the input device.

An illustration of the added capacitance along with an explanation of how this added capacitance affects the propagation delay follows:

Table V. Parametric Test Conditions - Dual D Flip-Flop

Test No.	Parameter	Bias Conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Units	Limits Min.	Limits Max.
1	I_{CC}	GND	GND		5.5 V*		GND	GND	GND			GND			GND	mA		2.4
2	I_{CC}	GND	GND	GND	5.5 V*	GND	GND	GND				GND				mA		2.4
3	I_{IN} "0" (8)				5.5 V				0.3 V			GND				mA		0.15
4	I_{IN} "0" (14)				5.5 V							GND			0.3 V*	mA		0.15
5	I_{IN} "0" (5)				5.5 V	0.3 V*		GND				GND				mA		0.15
6	I_{IN} "0" (3)	GND		0.3 V*	5.5 V							GND				mA		0.15
7	I_{IN} "0" (8)				5.5 V	GND			0.3 V*			GND				mA		0.30
8	I_{IN} "0" (14)			GND	5.5 V							GND			0.3 V*	mA		0.30
9	I_{IN} "0" (3)	GND	GND	0.3 V*	5.5 V							GND			GND	mA		0.15
10	I_{IN} "0" (5)				5.5 V	0.3 V*	GND	GND	GND			GND				mA		0.15
11	I_{IN} "0" (7)				5.5 V	GND		0.3 V*				GND				mA		0.15
12	I_{IN} "0" (9)	0.3 V*		GND	5.5 V							GND				mA		0.15
13	I_{IN} "0" (5)				5.5 V	0.3 V*	GND					GND				mA		0.15
14	I_{IN} "0" (3)		GND	0.3 V*	5.5 V							GND				mA		0.15
15	I_{IN} "1" (14)	MOM GND	2.4 V		5.5 V							GND			2.4 V*	µA		20
16	I_{IN} "1" (8)				5.5 V		2.4 V	MOM GND	2.4 V*			GND				µA		20
17	I_{IN} "1" (3)	GND	GND	2.4 V*	5.5 V							GND		MOM GND		µA		30
18	I_{IN} "1" (5)				5.5 V	2.4 V*	GND	GND		GND		GND				µA		30
19	I_{IN} "1" (6)				5.5 V	GND	2.4 V*					GND				µA		10

* Measured Line

Table V. (Continued)

Test No.	Parameter	Bias Conditions														Limits		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	Units	Min.	Max.
20	I_{IN} [1, 2]		2.4 V*	GND	5.5 V							GND				µA		
21	I_{IN} [3, 7]				5.5 V	GND		2.4 V*				GND				µA		20
22	I_{IN} [11, 14]	2.4 V*		GND	5.5 V							GND				µA		20
23	I_{IN} [11, 14]	MOM GND	2.4 V		5.5 V							GND			5.5 V*	µA		200
24	I_{IN} [8]				5.5 V		2.4 V	MOM GND	5.5 V			GND				µA		200
25	I_{IN} [13]	GND	GND	5.5 V*	5.5 V							GND		MOM* GND		µA		300
26	I_{IN} [5]				5.5 V	5.5 V*	GND	GND		MOM GND		GND				µA		300
27	I_{IN} [6]				5.5 V	GND	5.5 V*					GND				µA		100
28	I_{IN} [2]		5.5 V*	GND	5.5 V							GND				µA		100
29	I_{IN} [7]				5.5 V	GND		5.5 V*				GND				µA		200
30	I_{IN} [1]	5.5 V*		GND	5.5 V							GND				µA		200
31	I_{OUT} Leak [9]				5.0 V				GND	5.0 V*		GND				µA		250
32	I_{OUT} Leak [10]				5.0 V	GND					5.0 V*	GND				µA		250
33	I_{OUT} Leak [13]				5.0 V							GND		5.0 V*	GND	µA		250
34	I_{OUT} Leak [12]			GND	5.0 V							GND	5.0 V*			µA		250
35	I_{OS} [9]				5.5 V				GND	GND*		GND				mA	-3	-15
36	I_{OS} [10]				5.5 V	GND					GND*	GND				mA	-3	-15
37	I_{OS} [13]				5.5 V							GND		GND*	GND	mA	-3	-15
38	I_{OS} [12]			GND	5.5 V							GND	GND*			mA	-3	-15

* Measuring Line

Table V. (Concluded)

Test No.	Parameter	Bias Conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Units	Limit Min.	Limit Max.
39	V_{OUT} 0 10				4.5 V				GND		0.3 V*	GND				mA	2.0	
40	V_{OUT} 0 9				4.5 V	GND				0.3 V*		GND				mA	2.0	
41	V_{OUT} 0 12				4.5 V							GND	0.3 V*		GND	mA	2.0	
42	V_{OUT} 0 13			GND	4.5 V							GND		0.3 V*		mA	2.0	
43	V_{OUT} 1 9				4.5 V				0.7 V	-100 μA*		GND				Volts	2.4	
44	V_{OUT} 1 10				4.5 V	0.7 V					-100 μA*	GND				Volts	2.4	
45	V_{OUT} 11 13				4.5 V							GND		-100 μA	0.7 V	Volts	2.4	
46	V_{OUT} 11 12			0.7 V	4.5 V							GND	-100 μA			Volts	2.4	
47	I_{CLAMP} 1	-1 mA*			4.5 V							GND				Volts	-1.2Δ	
48	I_{CLAMP} 2		-1 mA*		4.5 V							GND				Volts	-1.2Δ	
49	I_{CLAMP} 3			-1 mA*	4.5 V							GND				Volts	-1.2Δ	
50	I_{CLAMP} 5				4.5 V	-1 mA*						GND				Volts	-1.2Δ	
51	I_{CLAMP} 6				4.5 V		-1 mA*					GND				Volts	-1.2Δ	
52	I_{CLAMP} 7				4.5 V			-1 mA*				GND				Volts	-1.2Δ	
53	I_{CLAMP} 8				4.5 V				-1 mA*			GND				Volts	-1.2Δ	
54	I_{CLAMP} 14				4.5 V							GND			- mA*	Volts	-1.2Δ	

* Measurement Sheet

Table VI. Parametric Test Conditions - Dual Four Nand Gate

Test No.	Parameter	Pin Conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Unit	Limits Min.	Limits Max.
1	I_{CC}	GND			5.5 V*		GND								GND	μA		-0.32
2	I_{CC} 0	5 V			5.5 V*		5 V	5 V	5 V	5 V					GND	μA		-0.44
3	I_{IN} 0 1	0.3 V*			5.5 V										GND	μA		-0.15
4	I_{IN} 0 6						0.3 V*								GND	μA		-0.15
5	I_X 0 3			0.3 V*	5.5 V										GND	μA		-0.18
6	I_Y 0 5				5.5 V	1.0 V									GND	μA		-0.18
7	I_{IN} 1 1	2.4 V*			5.5 V										GND	μA		10.0
8	I_{IN} 1 2	GND			5.5 V										GND	μA		10.0
9	I_{IN} 1 13	GND			5.5 V										GND	μA		10.0
10	I_{IN} 1 14	GND			5.5 V										GND	μA		10.0
11	I_{IN} 1 6				5.5 V		2.4 V*	GND	GND	GND					GND	μA		10.0
12	I_{IN} 1 7				5.5 V		GND	2.4 V*	GND	GND					GND	μA		10.0
13	I_{IN} 1 8				5.5 V		GND	GND	2.4 V*	GND					GND	μA		10.0
14	I_{IN} 1 9				5.5 V		GND	GND	GND	2.4 V*					GND	μA		10.0
15	I_{IN} B1 1	5.5 V*			5.5 V										GND	μA		100
16	I_{IN} B1 12	GND			5.5 V										GND	μA		100
17	I_{IN} B1 13	GND			5.5 V										GND	μA		100
18	I_{IN} B1 14	GND			5.5 V										GND	μA		100
19	I_{IN} B1 6				5.5 V		5.5 V*	GND	GND	GND					GND	μA		100

* Device Under

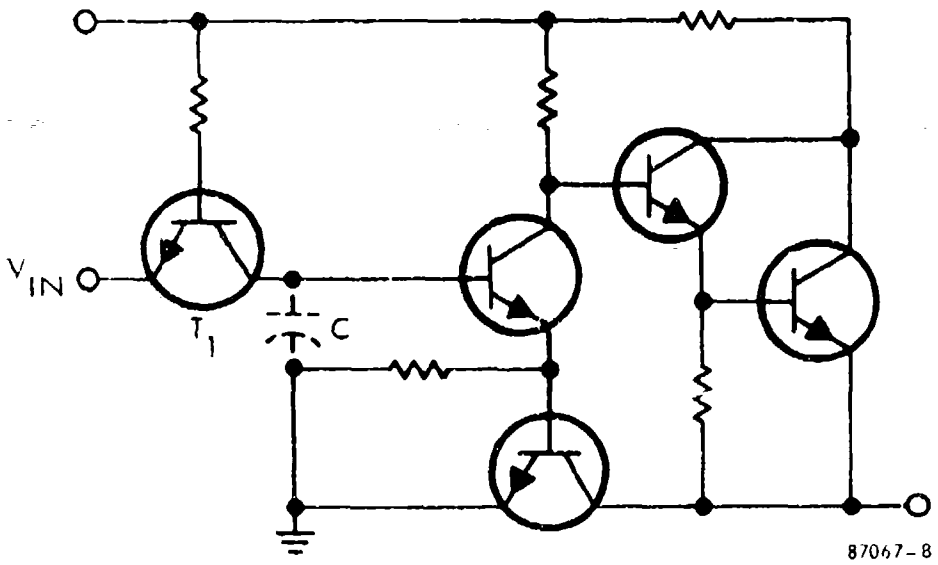
Table VI. (Continued)

Test No.	Parameter	Pin Connections														Limits		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	Units	Min.	Max.
20	I_{IL} B...				5.5 V		GND	5.5 V*	GND	GND		GND				µA		00
21	I_{IL} B...				5.5 V		GND		5.5 V*	GND		GND				µA		100
22	I_{IL} B...				5.5 V		GND	GND	GND	5.5 V*		GND				µA		100
23	V_{OUT} 0 2	2.0 V	-2 mA*		4.5 V							GND	2.0 V	2.0 V	2.0 V	Volts		0.3
24	V_{OUT} 0 10				4.5 V		2.0 V	2.0 V	2.0 V	2.0 V	-2 mA*	GND				Volts		0.3
25	V_{OUT} [illegible]	0.7 V	-100 µA*		4.5 V							GND				Volts	2.4	
26	V_{OUT} [illegible] 12		-100 µA*		4.5 V							GND	0.7 V			Volts	2.4	
27	V_{OUT} [illegible] 13		-100 µA*		4.5 V							GND		0.7 V		Volts	2.4	
28	V_{OUT} [illegible] 14		-100 µA*		4.5 V							GND			0.7 V	Volts	2.4	
29	V_{OUT} [illegible] 6				4.5 V		0.7 V				-100 µA*	GND				Volts	2.4	
30	V_{OUT} [illegible] 7				4.5 V			0.7 V			-100 µA*	GND				Volts	2.4	
31	V_{OUT} [illegible] 8				4.5 V				0.7 V		-100 µA*	GND				Volts	2.4	
32	V_{OUT} [illegible] 9				4.5 V					0.7 V	-100 µA*	GND				Volts	2.4	
33	V_{OUT} [illegible] 5			0.5 V	4.5 V						-100 µA*	GND				Volts	2.4	
34	V_{OUT} [illegible] 5				4.5 V	1.0 V					-100 µA*	GND				Volts	2.4	

Table VI. (Concluded)

Test No.	Parameter	Bias Conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Units	Limit Min.	Limit Max.
35	I_{OL} Lead 2	GND	5.0 V*		5.0 V							GND				µA		250
36	I_{OL} Lead 10				5.0 V		GND				5.0 V*	GND				µA		250
37	I_{CC} 2	GND	0 V*		5.0 V							GND				mA	-3.0	-15.0
38	I_{CC} 10				5.0 V		GND				0 V*	GND				mA	-3.0	-15.0
39	I_{IN} CLAMP	1 mA*			5.0 V							GND				Volts		-2.0 V
40	I_{IN} CLAMP				5.0 V		-1.0 mA*					GND				Volts		-2.0 V

* Sense Line



When the input is at a logical "0" level the voltage across the capacitor is:

$$V_C = V_{IN} + V_{OFFSET\ T_1}$$

The voltage across the capacitor must increase to 2 V_{BE}'s in order to turn on the output device.

The capacitance for an oxide dielectric capacitor is given below:

$$C = \frac{\epsilon A}{d}$$

$\epsilon_r = 3.9$

$\epsilon = \epsilon_r \epsilon_o$

$\epsilon_o = 8.83\ (10^{-12})$ f/m

$C/A = \epsilon/d$

$\epsilon = 34.5$ pF/m

$$C/A = \frac{34.5}{d}$$

where d is expressed in meters and C/A is pF/m^2

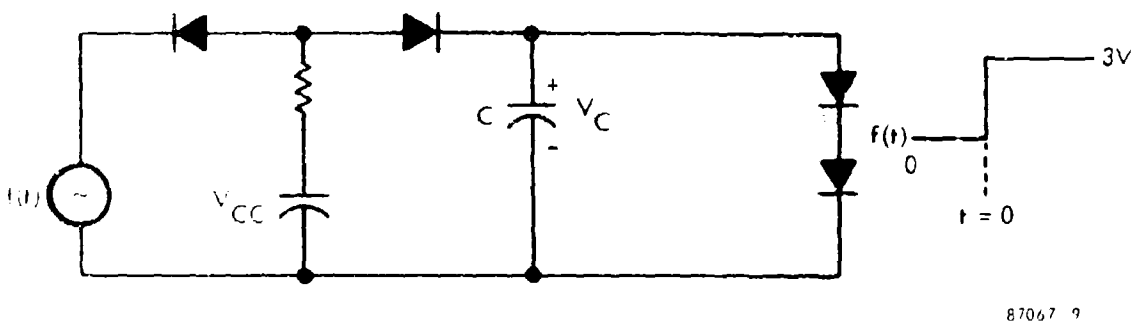
$$C/A = \frac{224}{d}$$

where d is expressed in Å and C/A is in pF/mil^2

For an oxide thickness of 10,000 Å

$$C/A = \frac{0.0224\ pF}{mil^2}$$

A simplified schematic is shown below:



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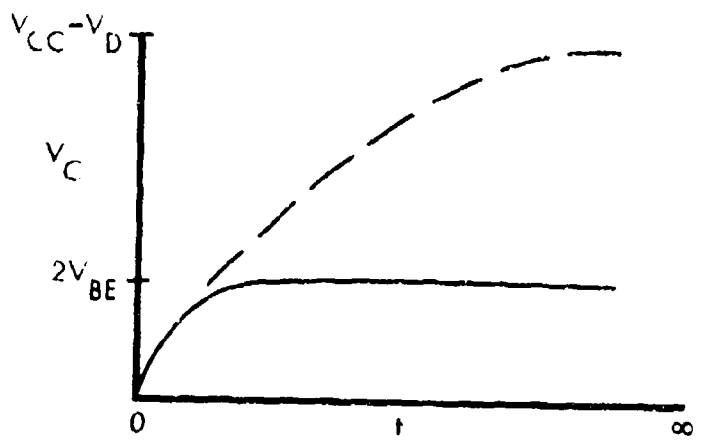
An expression of the voltage across the capacitor as a function of time is given below.

@ t = o $\qquad V_C = V_{IN} + V_{OFFSET}$

@ t = ∞ $\qquad V_C = 2V_{BE's}$



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$$V_C = 1/C \int i_C \, dt + V_{CO}$$

Q_o = initial charge on C

V_{CO} = initial voltage on C

$$V_{CC} - V_D - V_{CO} = R\, i_C + 1/C \int_{-\infty}^{t} i_C \, dt$$

$$\frac{V_{CC} - V_D - V_{CO}}{S} = RI(S) + 1/C \left[\frac{I(S)}{S}\right]$$

$$\left(\frac{1}{CS} + R\right) I(S) = \frac{1}{S} (V_{CC} - V_{CO} - V_D)$$

$$I(S) = \frac{(V_{CC} - V_{CO} - V_D)\, C}{1 + RCS}$$

$$I(S) = (V_{CC} - V_{CO} - V_D) \frac{C/RC}{S + 1/RC}$$

$$i(t) = \frac{(V_{CC} - V_{CO} - V_D)}{R} e^{-t/RC}$$

$$i(t)\, R = (V_{CC} - V_{CO} - V_D)\, e^{-t/RC}$$

when $i(t)\, R = (V_{CC} - 3\, V_{BE's})$

then $V_C = 2\, V_{BE's}$

substituting values

$$5 - 2.1 = (5 - 0.8)\, e^{-t/RC}$$

$$2.9 = 4.2\, e^{-t/RC}$$

$$.69 = e^{-X}$$

$$X = 0.502$$

$$t = (0.502)\ RC$$

$$R = 40\ k\Omega$$

$A = 3.4\ mil^2$ = area of interconnect passing over the cross under.

$$C = \frac{224\ pF\ 3.4\ mil^2\ pF}{2\ (10^3)\ mil^2}$$

$$C = 0.380\ pF$$

$$t = (0.502)\ 4\ (10^4)\ (0.38)\ (10^{-12})$$

$$t = 7.6\ ns$$

Although no concrete conclusion was reached as to the reason for the discrepancy between the empirical and analytical results, it is believed to be attributable to the constant used to define the capacitance per unit area.

Except for this minor disagreement, it can be concluded that the electrical performance did meet and exceed the design goals set.

SECTION VI

CHARACTERIZATION

6.0 GENERAL

The purpose of this section is to provide the results of the characterization of both the Dual D Flip-Flop and the Dual Four Nand Gate over the operating temperature range of -55° C to +125° C. Included also will be plots of some of the more important parameters showing the graphic variation of the parameters over temperature.

6.1 DUAL D FLIP-FLOP

Table VII tabulates the DC characterization data for the device while Table VIII tabulates the AC characterization data. Figures 22 through 26 are the plots over temperatures for the parameters I_{CC}, I_{IN}, and V_{OUT}.

6.2 DUAL FOUR NAND GATE

Table IX tabulates the DC characterization data for the Dual Gate device while Table X tabulates the AC characterization data. Figures 27 through 30 provide a graphical presentation of the variation of the parameters I_{CC}, V_{OUT}, and I_{IN} over the operating temperature range. Figures 31 through 33 show plots of the gate transfer curves for variations in supply voltage at each of the temperature extremes and room temperature.

Table VII. DC Characterization - Dual D Flip-Flop

Parameter	Temp. (° C)	Min.	Typ.	Max.	Limit
I_{CC}	- 55	1.80	2.0	2.2	
	25	1.80	1.9	2.15	<2.4 mA
	+125	1.87	2.1	2.25	
I_{IN} "0"	- 55	0.11	0.13	0.14	
	25	0.11	0.12	0.14	<0.15 mA
	+125	0.12	0.13	0.13	
I_{IN} "1"	- 55	3.2	3.5	4.0	
	25	3.5	4.5	6.2	<10 μA
	+125	5.4	6.9	10.0	
I_{OUT} Leakage	- 55	1.0	2.5	4.7	
	25	1.2	1.7	7.2	<250 μA
	+125	2.1	2.5	12.5	
I_{OS}	- 55	8.5	8.8	9.1	
	25	8.3	8.6	9.0	$3 < I_{OS} < 15$ mA
	+125	7.8	8.5	8.9	
I_{OUT} "0"	- 55	4.1	6.0	8.0	
	25	6.5	8.5	9.8	>2 mA
	+125	4.5	6.0	9.3	
V_{OUT} "1"	- 55	2.4	2.8	3.1	
	25	3.0	3.15	3.2	>2.4 V
	+125	3.1	3.4	3.5	
V_{CLAMP}	- 55	0.83	0.86	0.89	
	25	0.71	0.76	0.78	<1.2 V
	+125	0.56	0.60	0.63	

Table VIII. AC Characterization - Dual D Flip-Flop

Parameter	Temp. (° C)	Min.	Typ.	Max.	Units and Notes
Minimum clock pulse width	- 55	47	54	66	ns
	25	38	41	46	
	+125	29	31	32	
Setup time	- 55	8	18	28	ns
	25	7.5	14	18	
	+125	1.0	2.5	3	
Hold time	- 55	4	6	8	
	25	4	4.5	4.7	
	+125	1.0	2.0	2.8	
Propagation delay - t_{pd} "0"	- 55	98	116	135	ns
	25	72	78	92	
	+125	57	62	64	
Propagation delay - t_{pd} "1"	- 55	55	63	73	ns
	25	45	55	62	
	+125	39	44	50	
Reset propagation delay - t_{pd} "0"	- 55	71	77	84	ns
	25	51	55	59	
	+125	49	51	54	
Reset propagation delay - t_{pd} "1"	- 55	24	25	27	ns
	25	22	24	25	
	+125	25	27	30	
Set propagation delay - t_{pd} "0"	- 55	79	87	97	ns
	25	58	62	66	
	+125	50	53	56	
Set propagation delay - t_{pd} "1"	- 55	25	27	29	ns
	25	22	27	29	
	+125	26	27	32	

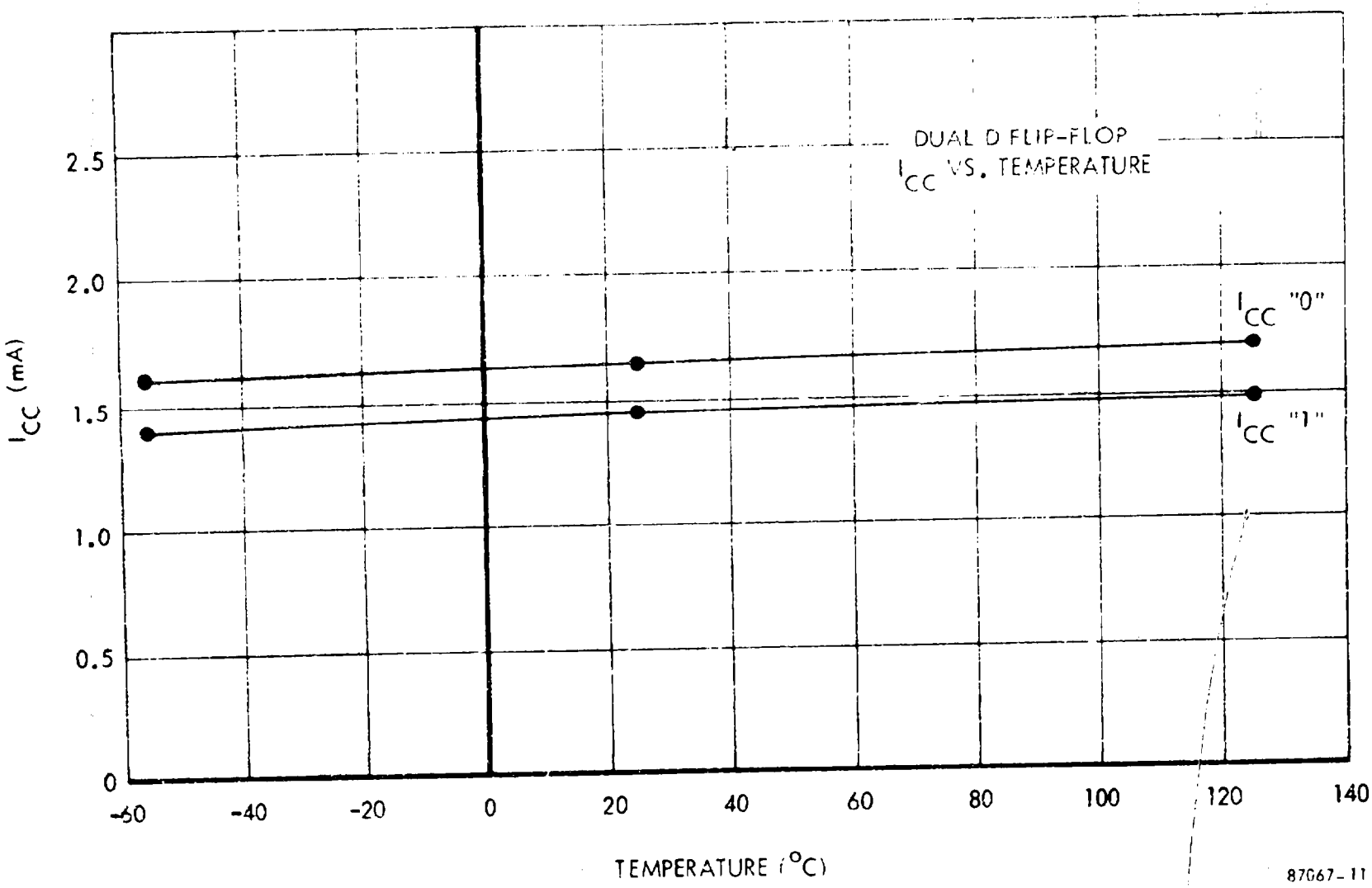


Figure 22. I_{CC} versus Temperature (Flip-Flop)

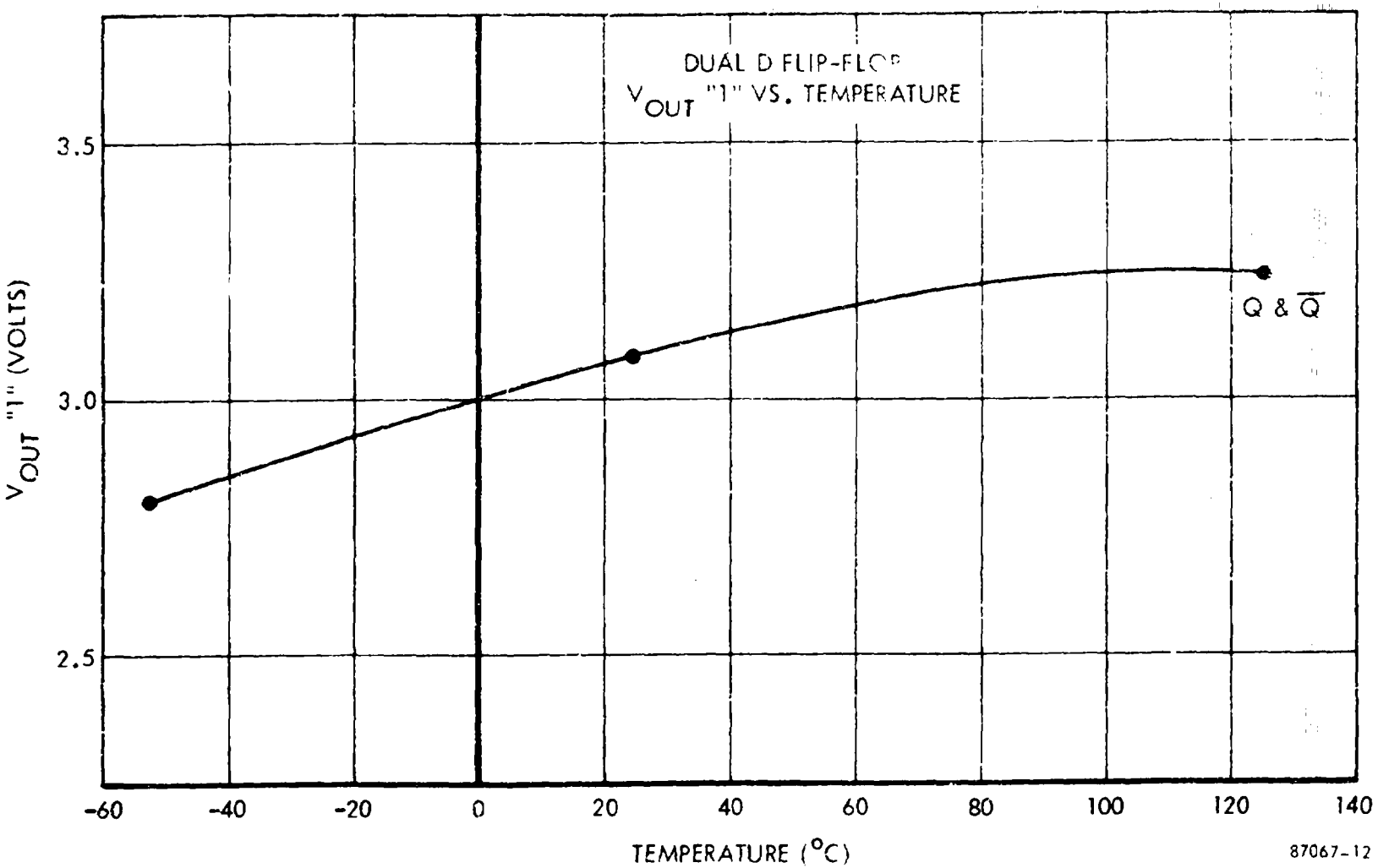


Figure 23. V_{OUT} "1" versus Temperature (Flip-Flop)

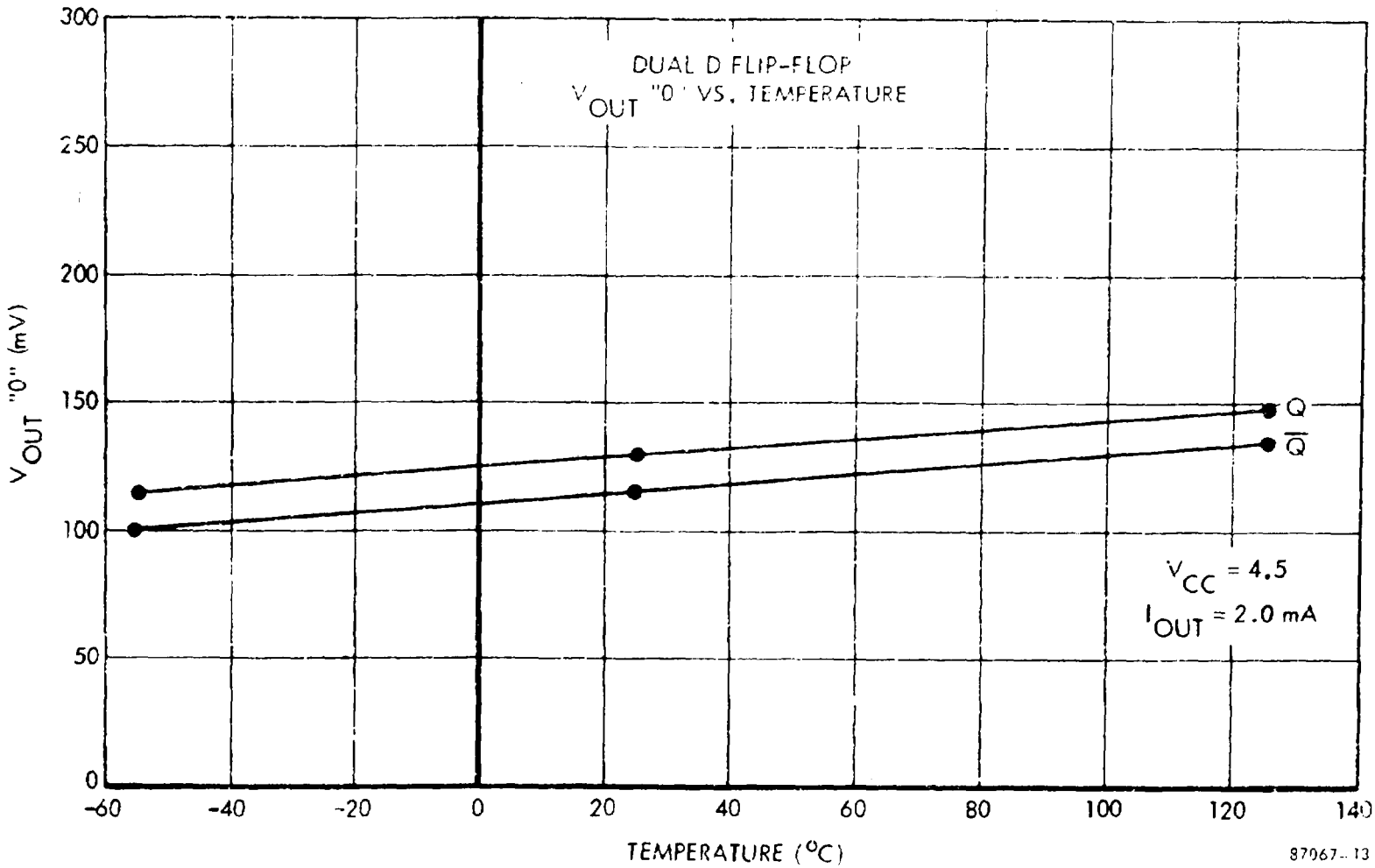


Figure 24. V_{OUT} "0" versus Temperature (Flip-Flop)

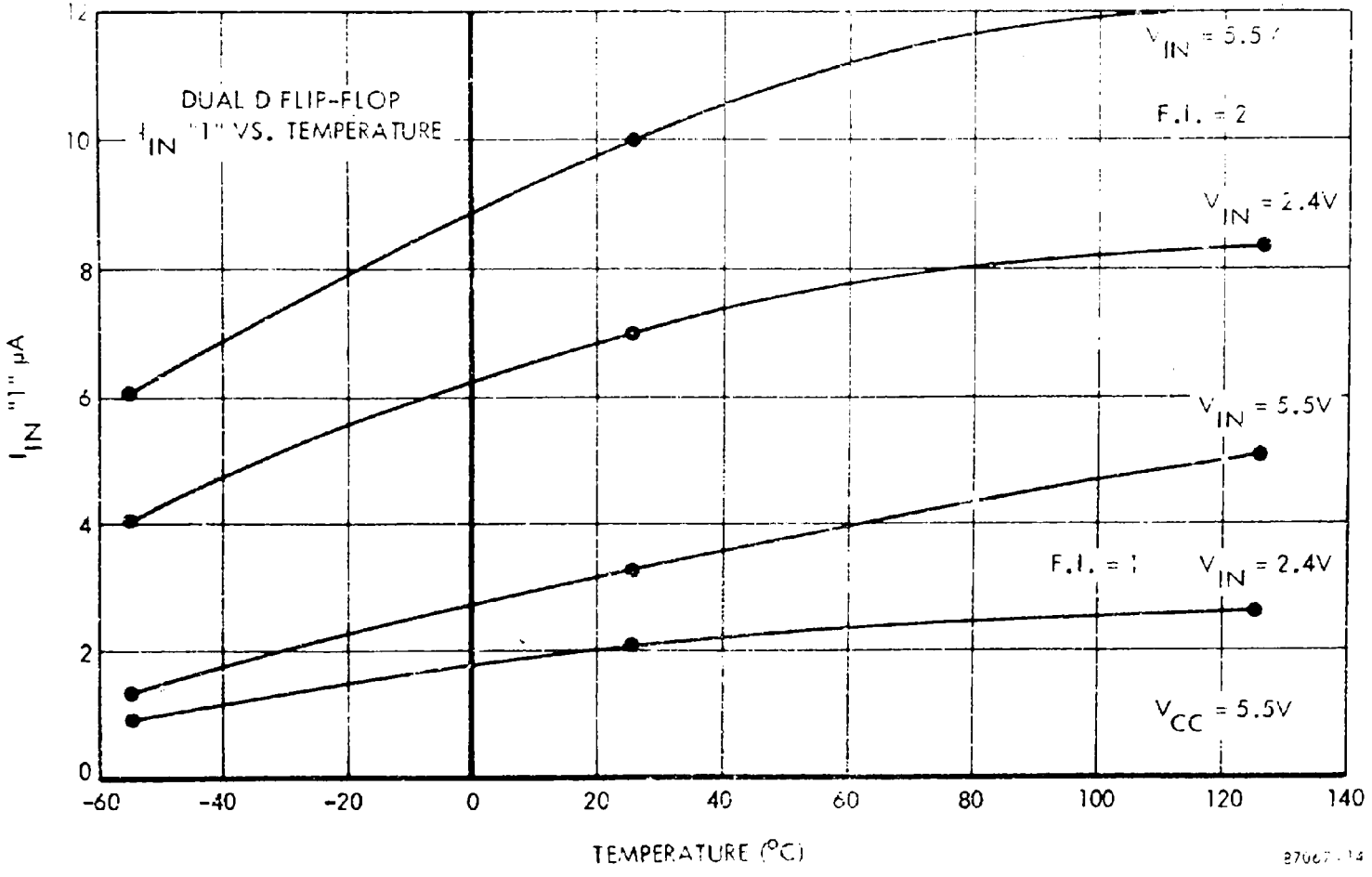


Figure 25. I_{IN} "1" versus Temperature (Flip-Flop)

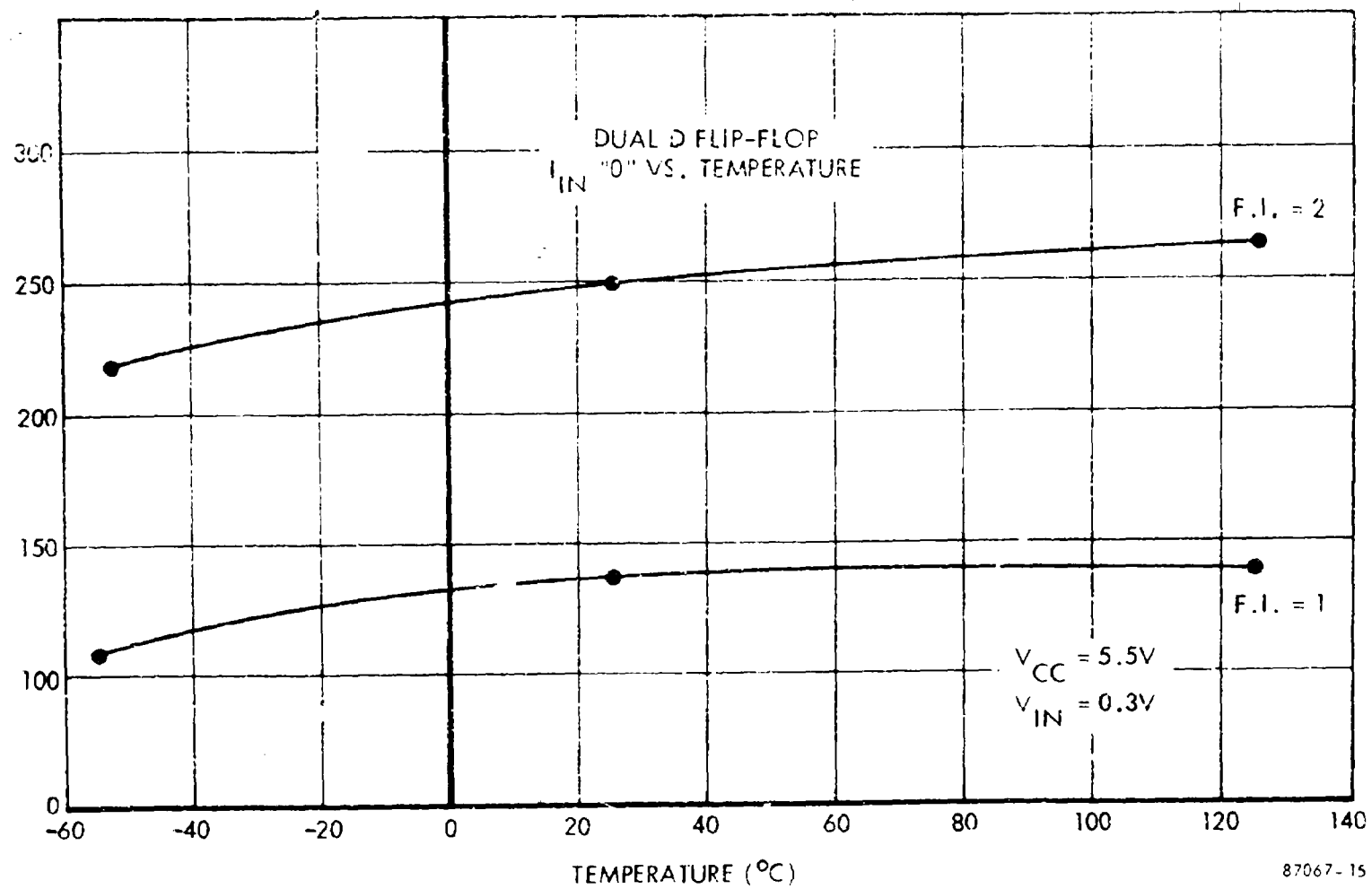


Figure 26. I_{IN} "0" versus Temperature (Flip-Flop)

Table IX. DC Characterization - Dual Four Nand Gate

Parameter	Temp. (° C)	Min.	Typ.	Max.	Limit
I_{CC} "1"	- 55	260	285	296	
	25	259	283	294	<320 μA
	+125	259	287	297	
I_{CC} "0"	- 55	685	750	792	
	25	698	760	808	<840 μA
	+125	728	780	835	
I_{IN} "0"	- 55	122	132	139	
	25	122	135	138	<150 μA
	+125	122	137	144	
I_{IN} "1" @ 2.4 V	- 55	5.0	5.2	7	
	25	5.2	6.2	8.2	<10 μA
	+125	7.3	8.8	10 μA	
I_{IN} "1" @ 5.5 V	- 55	8.1	10.1	13.4	
	25	10.3	15	17.4	<100 μA
	+125	13.3	18	20.5	
V_{OUT} "0"	- 55	123	135	140	
	25	137	149	160	<300 mV
	+125	150	190	212	
V_{OUT} "1"	- 55	2.68	2.84	2.92	
	25	2.91	3.03	3.14	>2.4 V
	+125	3.03	3.11	3.16	
V_{OUT} leakage	- 55	0	1	175	
	25	0	1	6.1	<250 μA
	+125	0	2	6.5	
I_{OS}	- 55	7.15	8.0	9.0	
	25	7.1	8.1	9.1	$-3<I_{OS}<-15$
	+125	7.2	8.1	9.1	
V_{CLAMP}	- 55	0.985	0.99	1.0	
	25	0.880	0.89	0.914	-2.0 V
	+125	0.762	0.78	0.832	

Table X. AC Characterization - Dual Four Nand Gate

Parameter	Temp. (° C)	Min.	Typ.	Max.	Limit (ns)
t_{pd} "0"	- 55	33.1	44	46.4	
	25	29.1	31	35.4	75
	+125	17.1	18.6	29.4	
t_{pd} "0"	- 55	60.9	69	75	
Extender	25	48.9	51	58.5	75
	+125	29.7	33	36.9	
t_{pd} "1"	- 55	19.1	21.6	28.5	
	25	19.5	21.1	27.8	60
	+125	21.0	23.4	27.8	
t_{pd} "1"	- 55	21.0	23.0	30.9	
Extender	25	21.0	22.3	26	60
	+125	22.4	23.3	27.0	

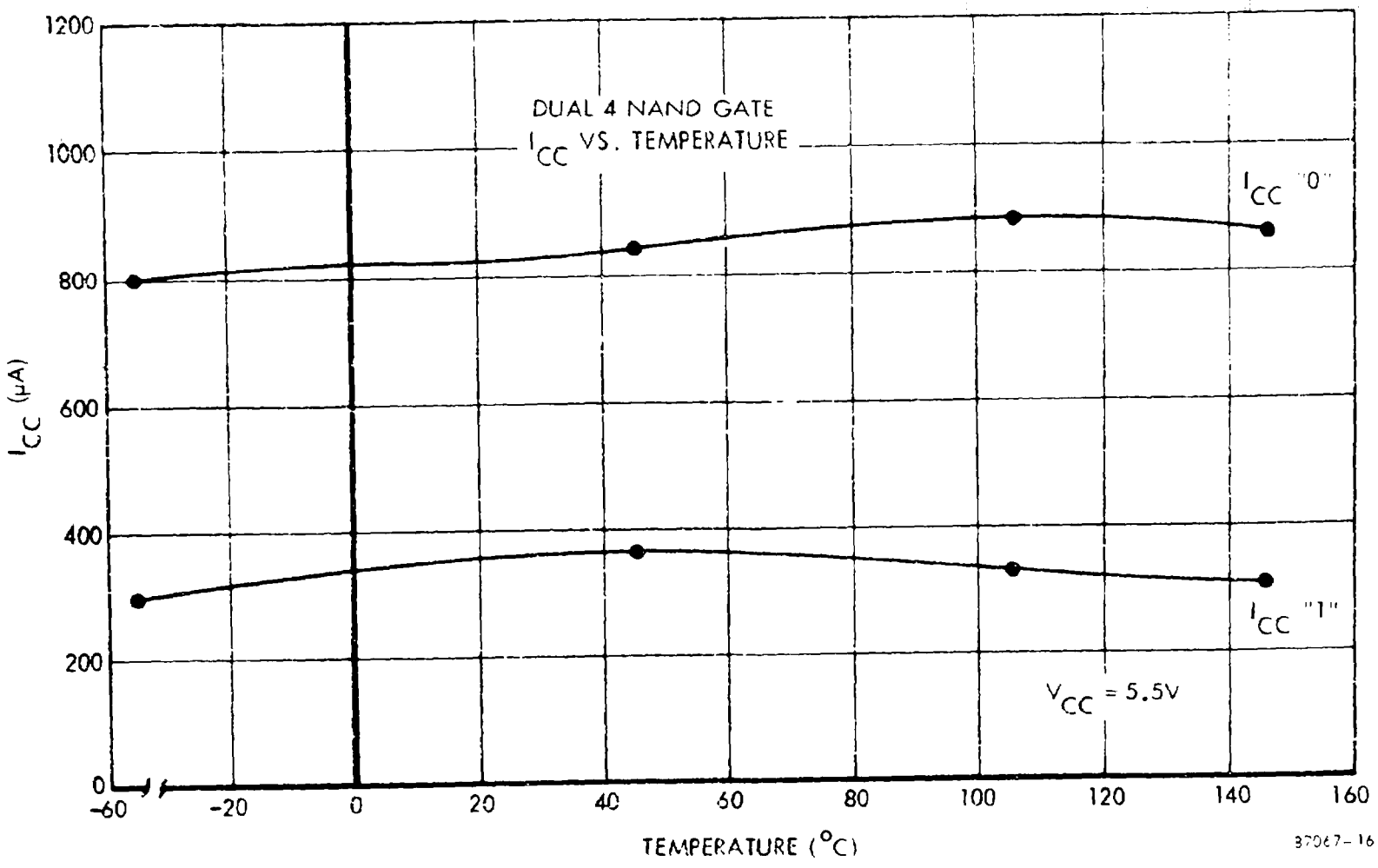


Figure 27. I_{CC} versus Temperature (Dual 4 Gate)

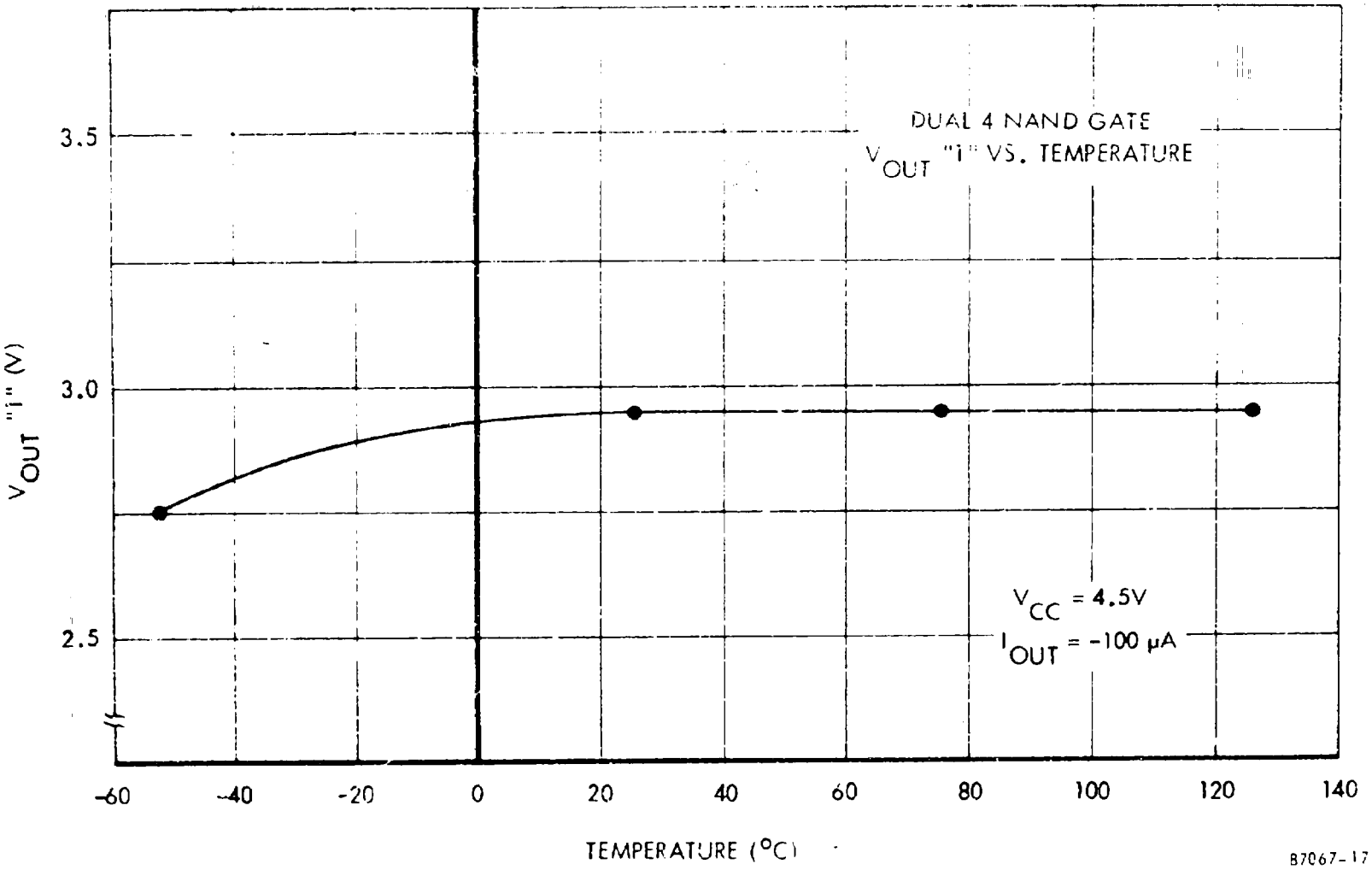


Figure 28. V_{OUT} "1" versus Temperature (Dual 4 Gate)

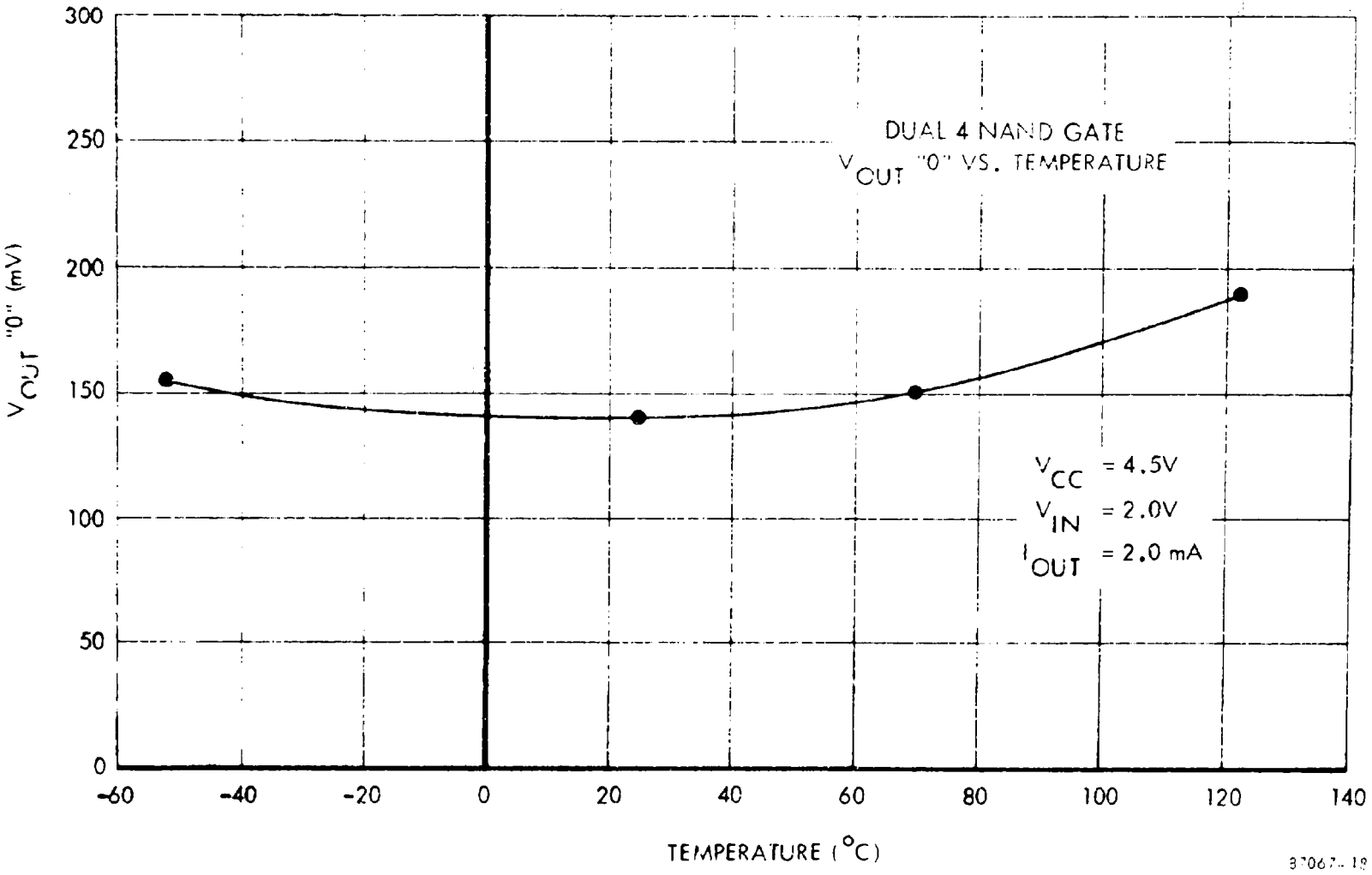


Figure 29. V_{OUT} "0" versus Temperature (Dual 4 Gate)

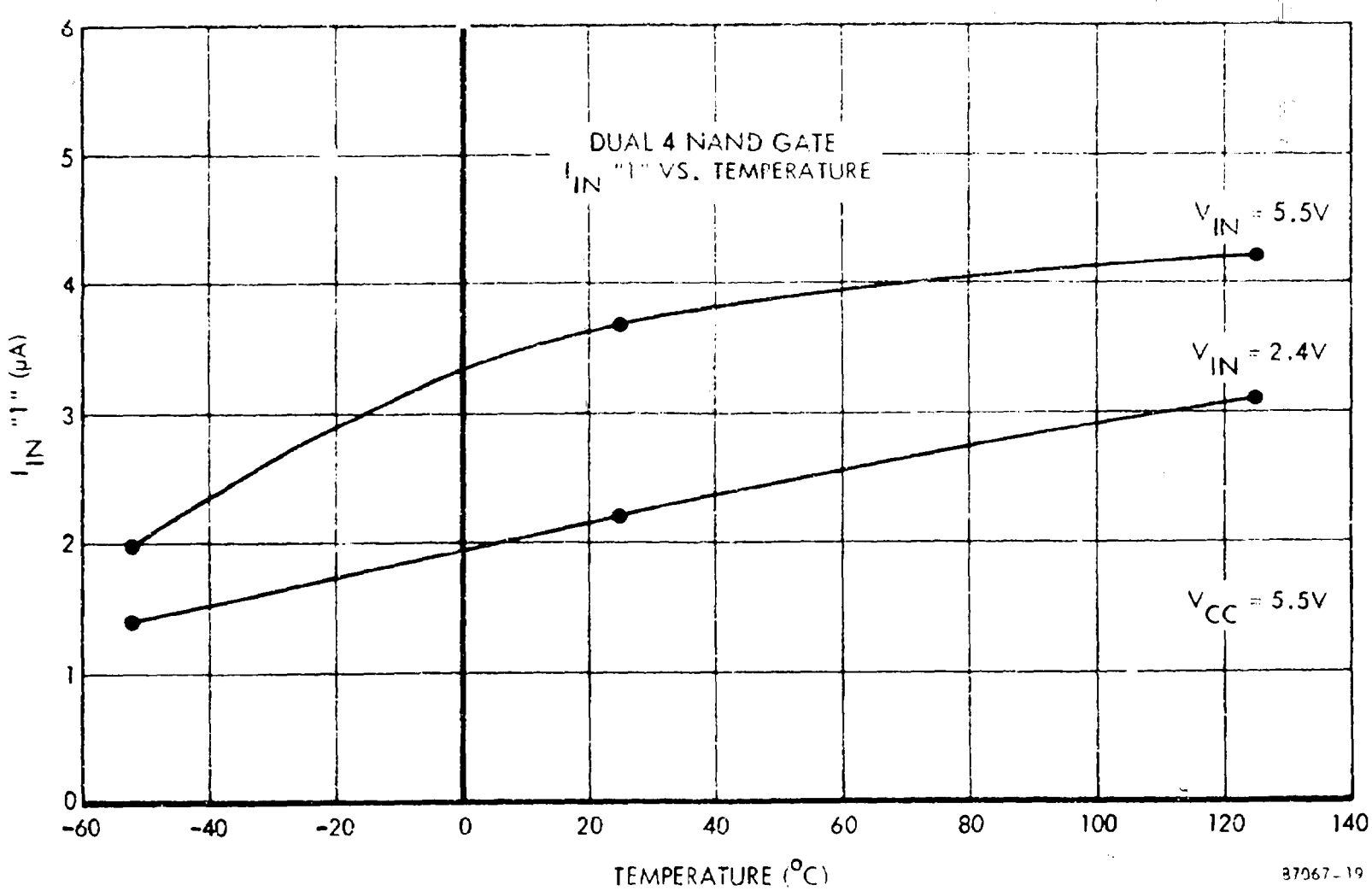


Figure 30. I_{IN} "1" versus Temperature (Dual 4 Gate)

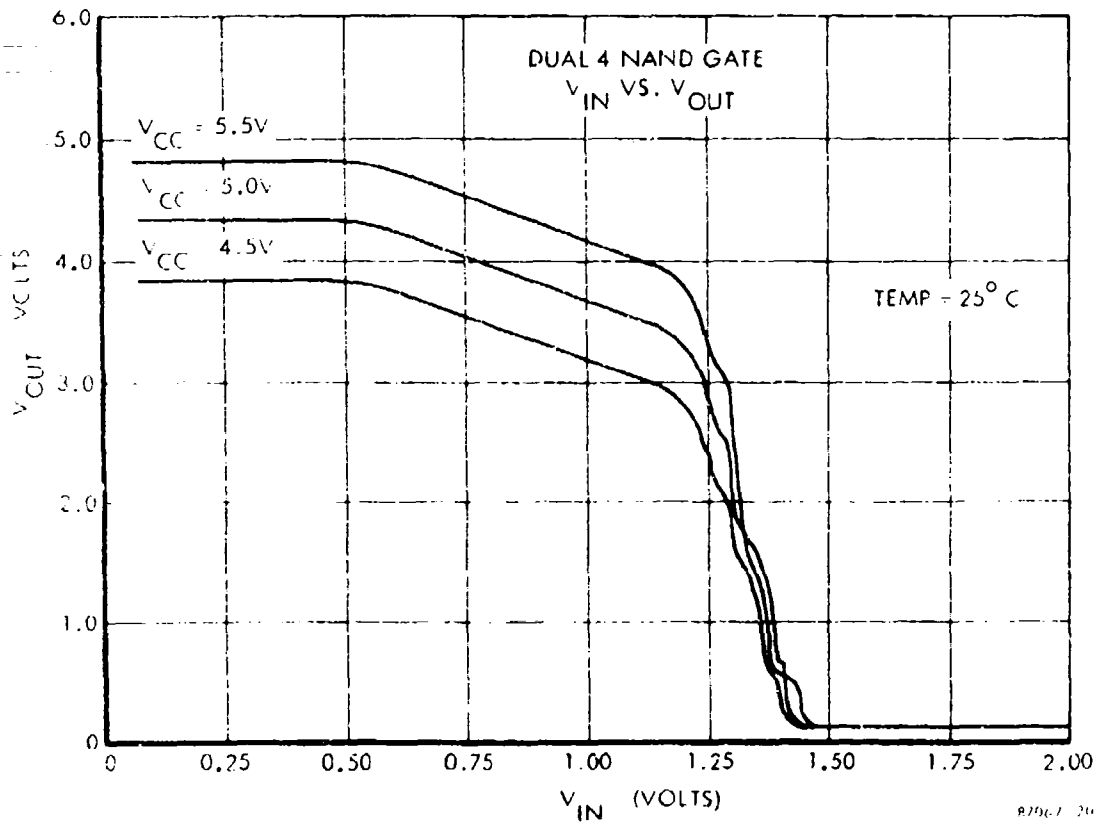


Figure 31. V_{IN} versus V_{OUT} (Dual 4 Gate)

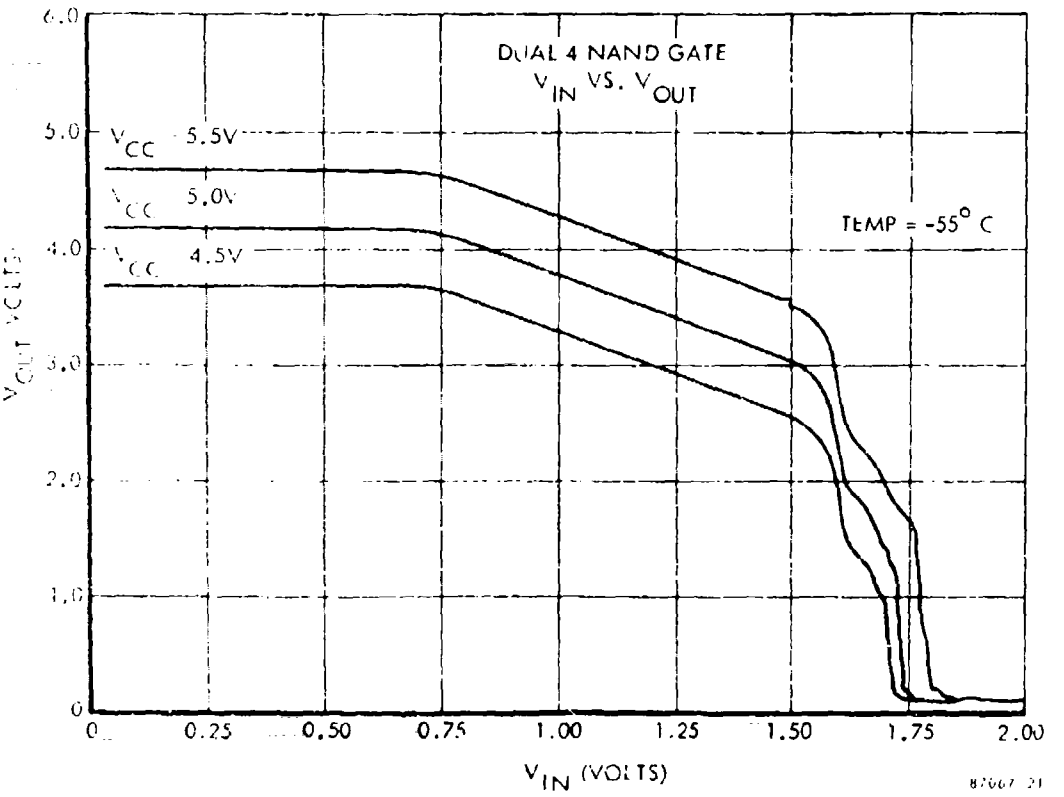


Figure 32. V_{IN} versus V_{OUT} (Dual 4 Gate)

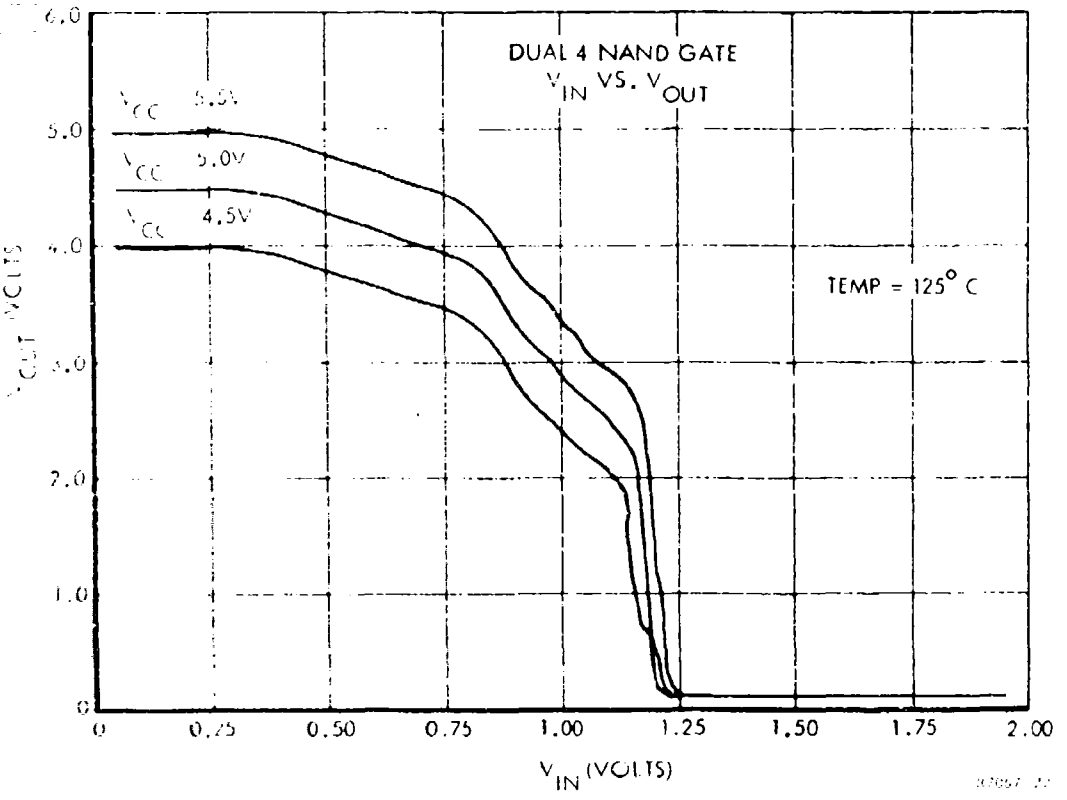


Figure 33. V_{IN} versus V_{OUT} (Dual 4 Gate)

SECTION VII

RELIABILITY STUDIES

7.0 GENERAL

Results of the reliability studies for Phase I and Phase II are presented in this section.

7.1 CHROME SILICON RESISTOR EVALUATION

An extensive reliability evaluation was conducted using the resistors produced during the development program. Many resistors having resistivities of 1.5 kΩ - 2.5 kΩ per square were life tested at +125° C for 1000 hours. A graph of the delta resistance distribution for one of the lots used in the test is shown in Figure 34 for 168,500 and 1,000 hours.

7.2 DEVICE EVALUATION

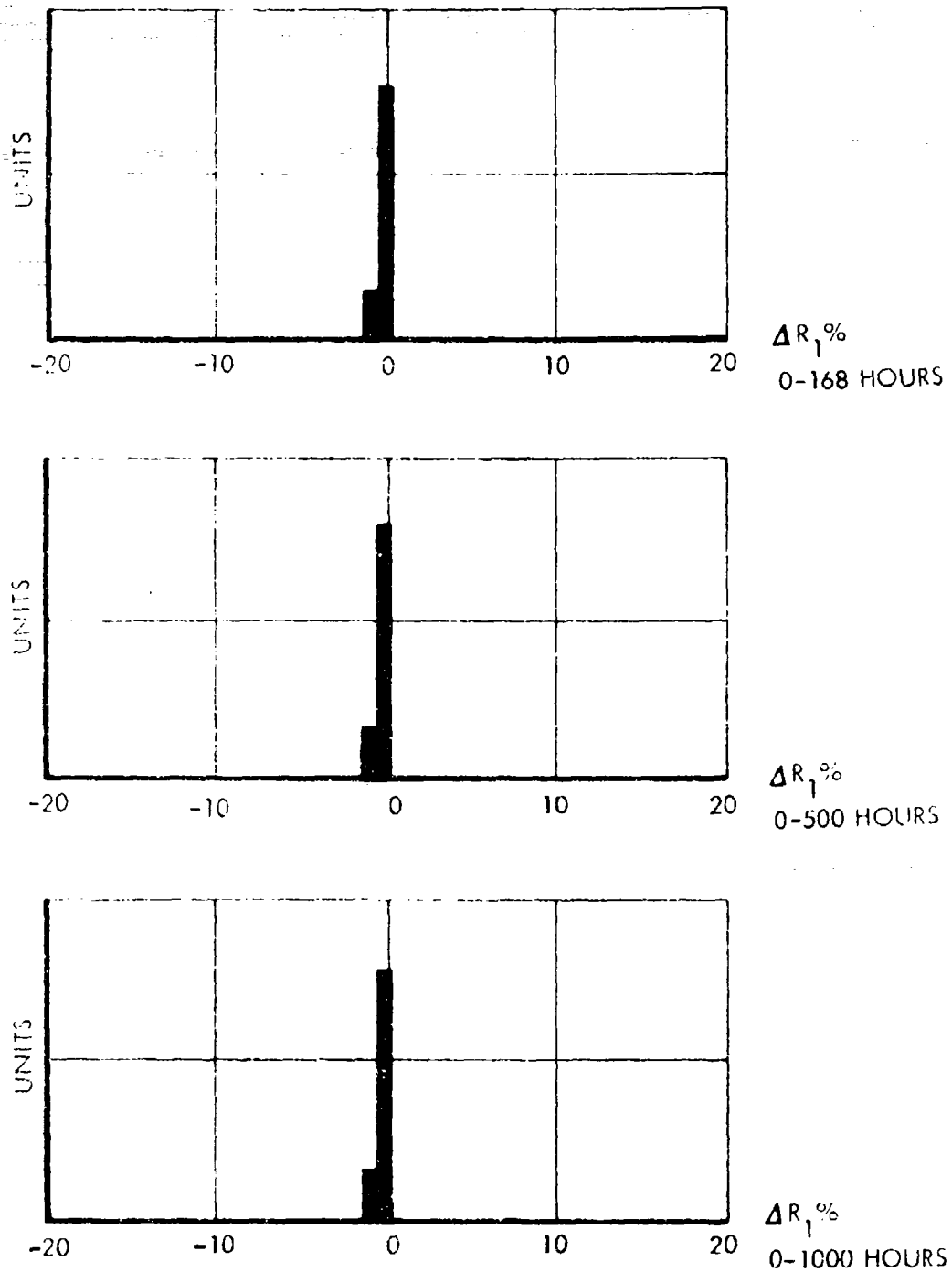
To further prove the stability of the chrome silicon thin film resistors, extensive operating and storage life test data was compiled on the flip-flop and dual gate.

From the data compiled on the sampled units from both Phase I and Phase II of the project, it can be concluded that the stability of the chrome-silicon resistors is outstanding (<±5%). Data will be presented in the succeeding sections to support this claim.

Table XI is a brief summary of the operating and storage life tests comparing the data results of Phase I product with Phase II product.

Table XI. Life Test Data Comparison

Test	Phase I		Phase II	
	2/4 Gate	Dual D F.F.	2/4 Gate	Dual D F.F.
Operating Life				
Sample size	12	12	24	24
Test duration	1,000 hrs.	1,000 hrs.	1,000 hrs.	1,000 hrs.
Circuit hours	12,000 hrs.	12,000 hrs.	24,000 hrs.	24,000 hrs.
Failures	0	0	0	0
Storage Life				
Samples size	10	10	20	22
Test duration	1,000 hrs.	1,000 hrs.	1,000 hrs.	1,000 hrs.
Circuit hours	10,000 hrs.	10,000 hrs.	20,000 hrs.	22,000 hrs.
Failures	0	0	0	0



CrSi RESISTOR
RUN 420X 1.5 kΩ/□
N = 18 T_A = +125° C

97067-23

Figure 34. Resistor Change versus Time (Operating Life)

7.2.1 DETAIL SUMMARY

The information presented in this section is presented in the form of histograms and/or scatter plots. The plots represent the data compiled on samples of the two type devices manufactured during Phase II of the program. Table XII is a [illegible]ation of the specific lots under test and the results of the tests conducted.

All data presented herewithin was compiled using test conditions described in Reliability Test Plan P 26 Revision 0 (previously supplied to Wright-Patterson). Data was taken at 0, 168, 500, and 1000 hours.

7.2.1.1 Dual D Flip-Flop

Figures 35 through 39 provide statistical operating life test data in the form of histograms and scatter plots for the two life test lot numbers specified in Table XII. Histogram data is provided for the parameters I_{IN} and V_{OUT}. Scatter plots are provided for I_{IN}, I_{OUT} and I_{OS}. Figures 40 through 44 summarize the storage life test data.

7.2.1.2 Dual Four Nand Gate

Figures 45 through 49 provide statistical operating life test data in the form of histograms and scatter plots for the two life test lot numbers specified in Table XII. Histogram data is provided for the parameters I_{IN} and V_{OUT}. Scatter plots are provided for I_{IN}, I_{OUT} and I_{OS}. Figures 50 through 54 summarize the storage life test data.

Table XII. Life Test Data on Phase II Product

L.T. No.	Circuit Type	Type of Test	Sample Size	Hours/ Failures
BL53	2/4 Gate	Operating	24	1000/0
BL53	2/4 Gate	Storage (+175° C)	20	1000/0
BL23	Dual D F.F.	Operating	24	1000/0
BL23	Dual D F.F.	Storage (+175° C)	22	1000/0

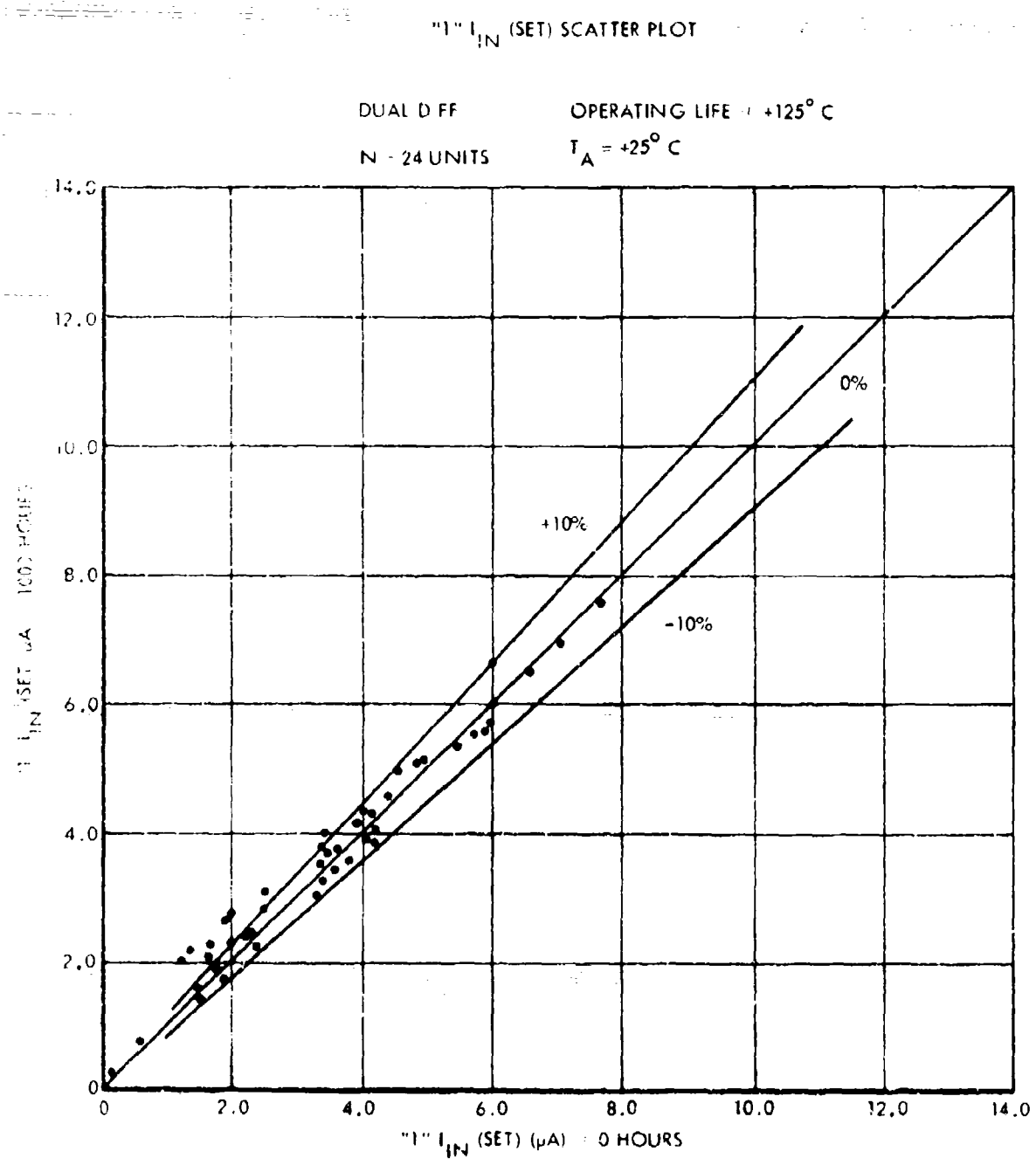


Figure 35. "1" I_{IN} (Set) Scatter Plot (Flip-Flop)

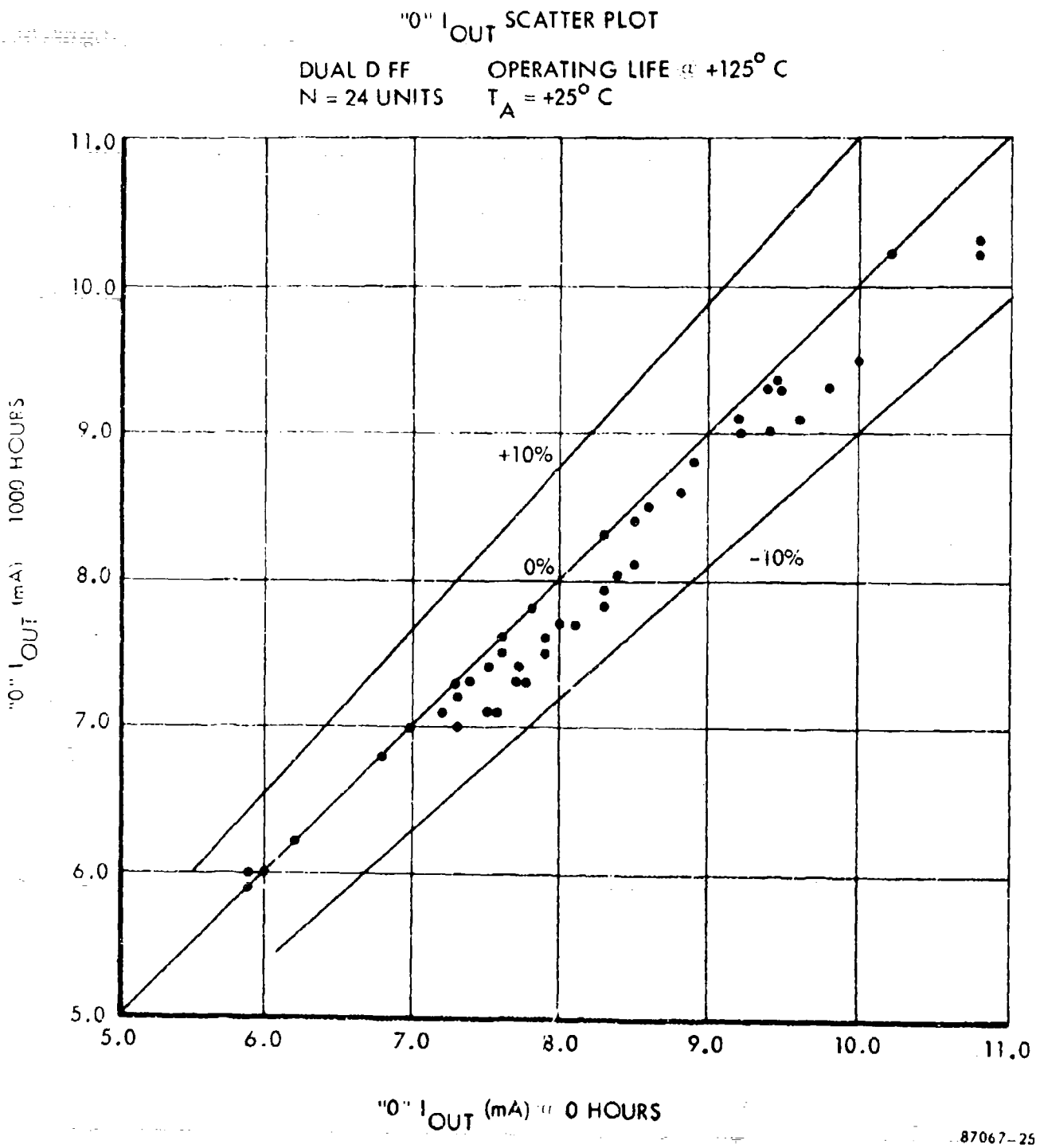


Figure 36. "0" I_{OUT} Scatter Plot (Flip-Flop)

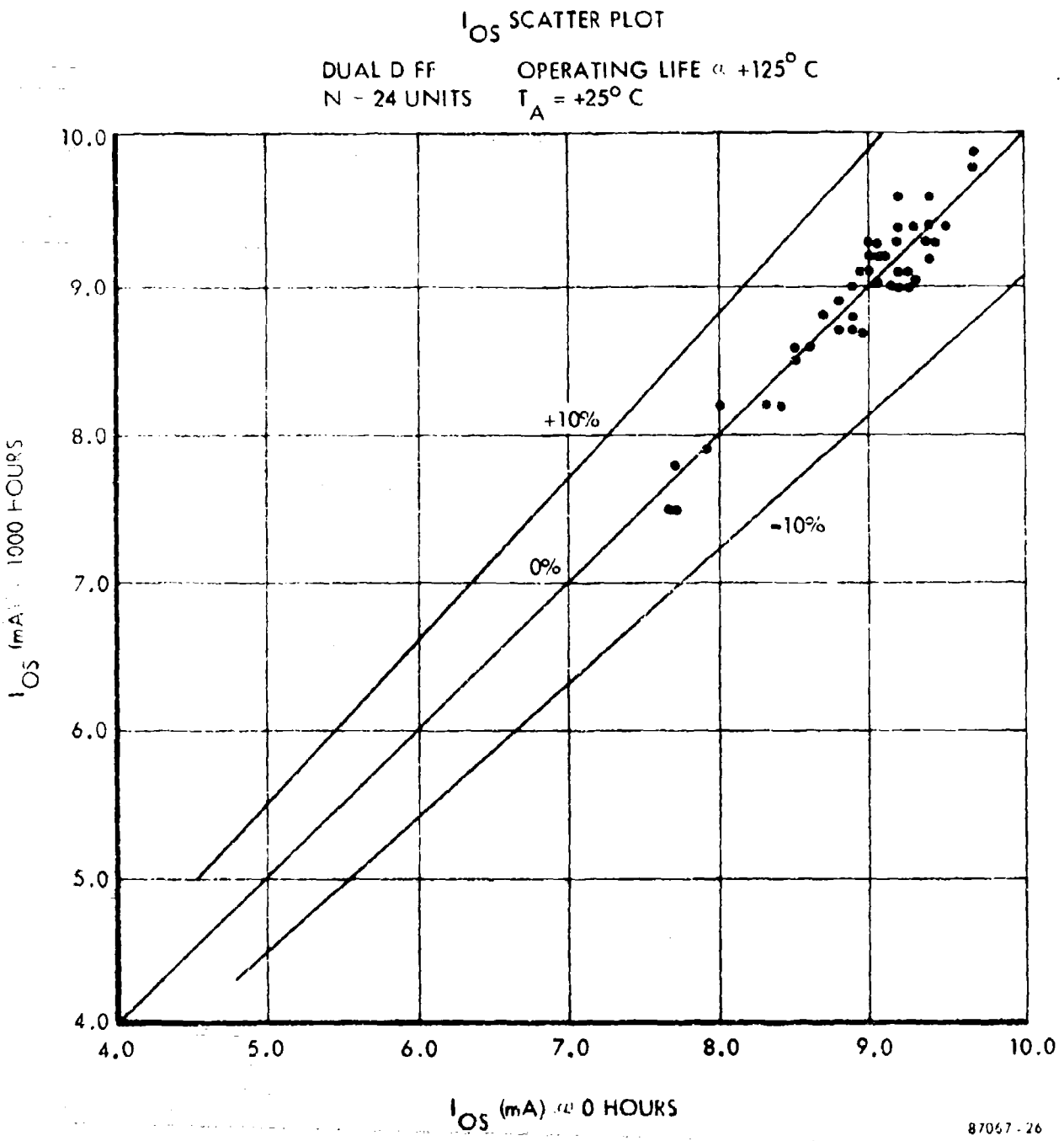


Figure 37. I_{OS} Scatter Plot (Flip-Flop)

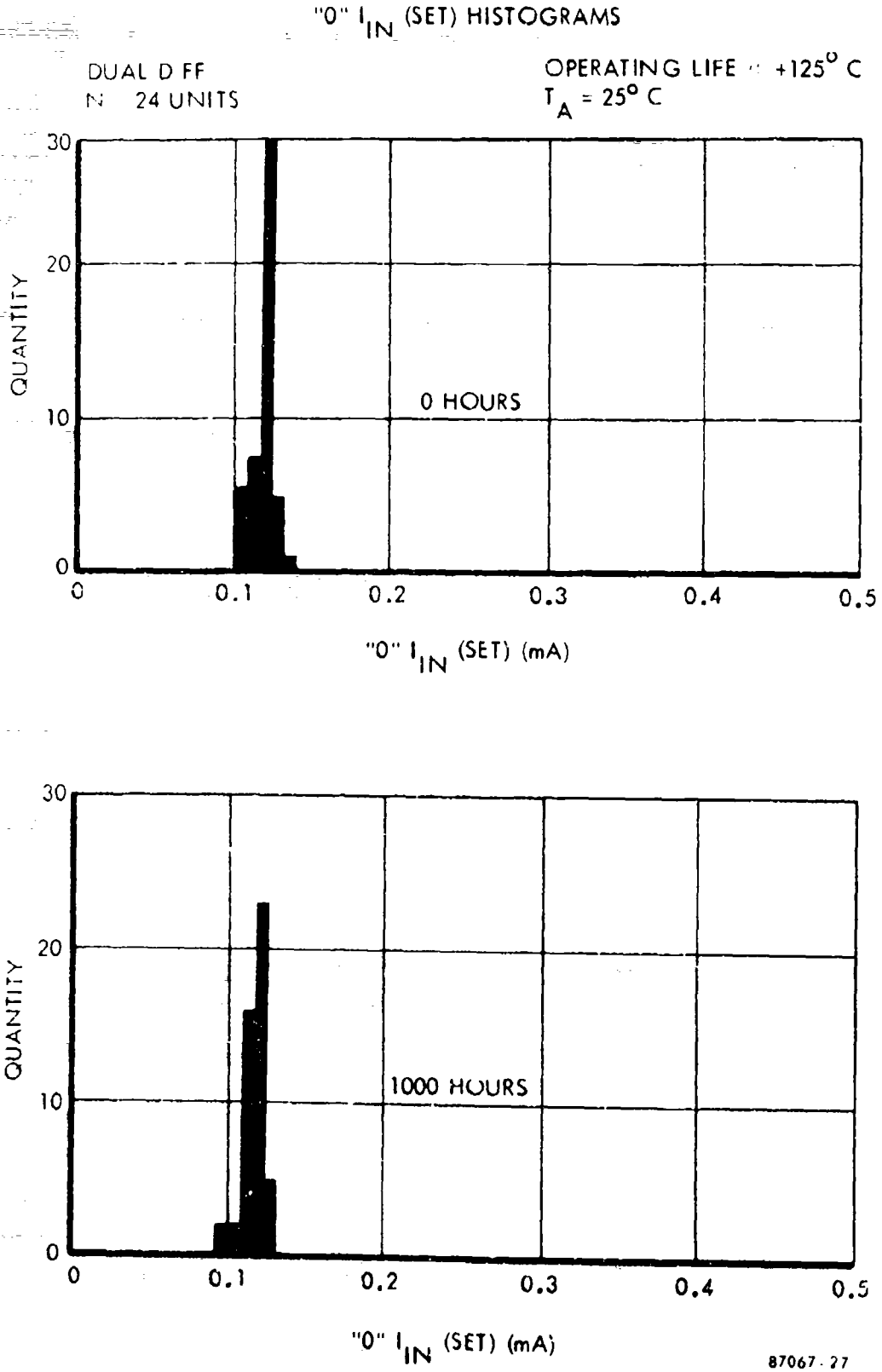


Figure 38. "0" I_{IN} (Set) Histograms (Flip-Flop)

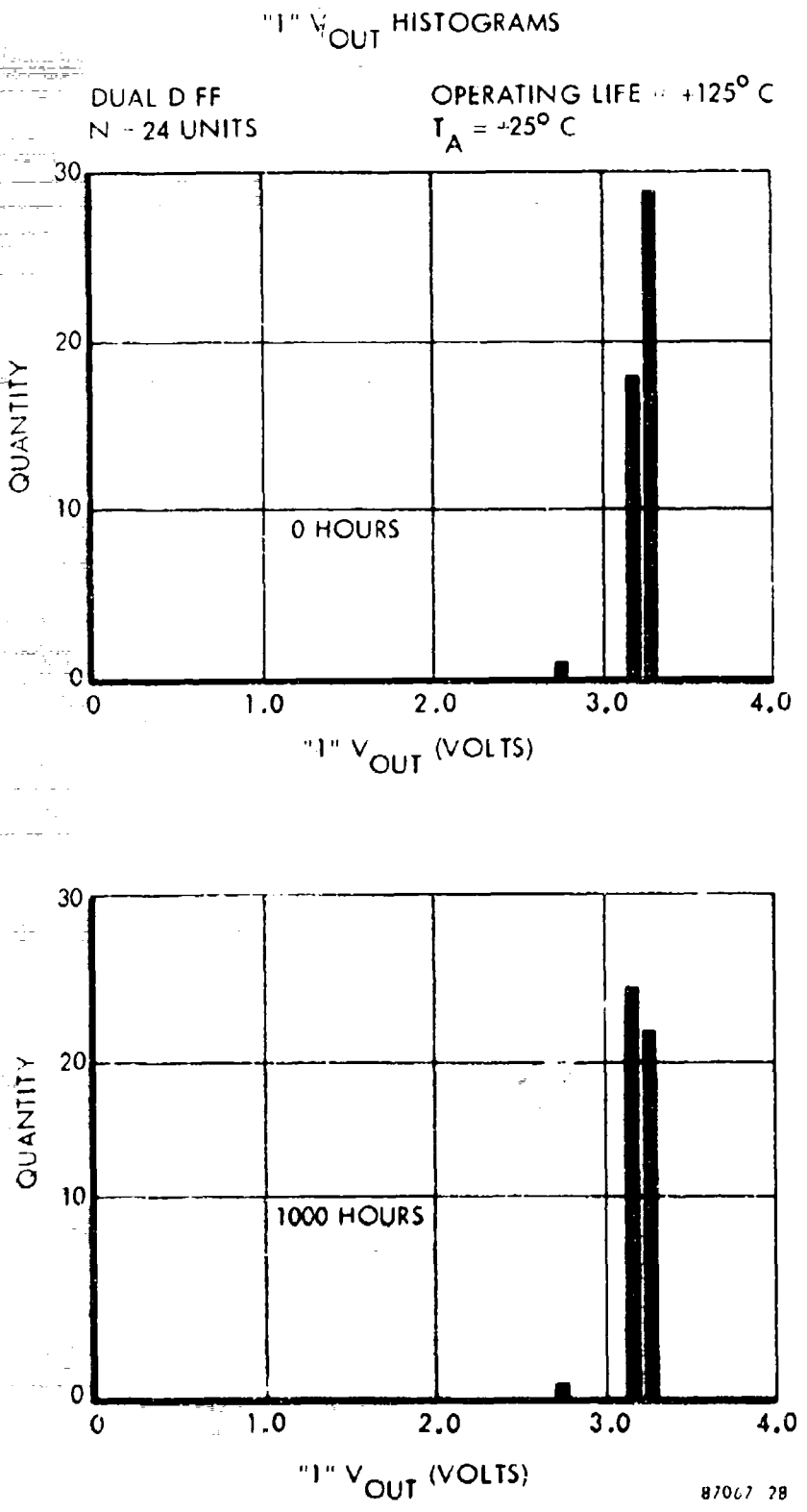


Figure 39. "1" V_{OUT} Histograms (Flip-Flop)

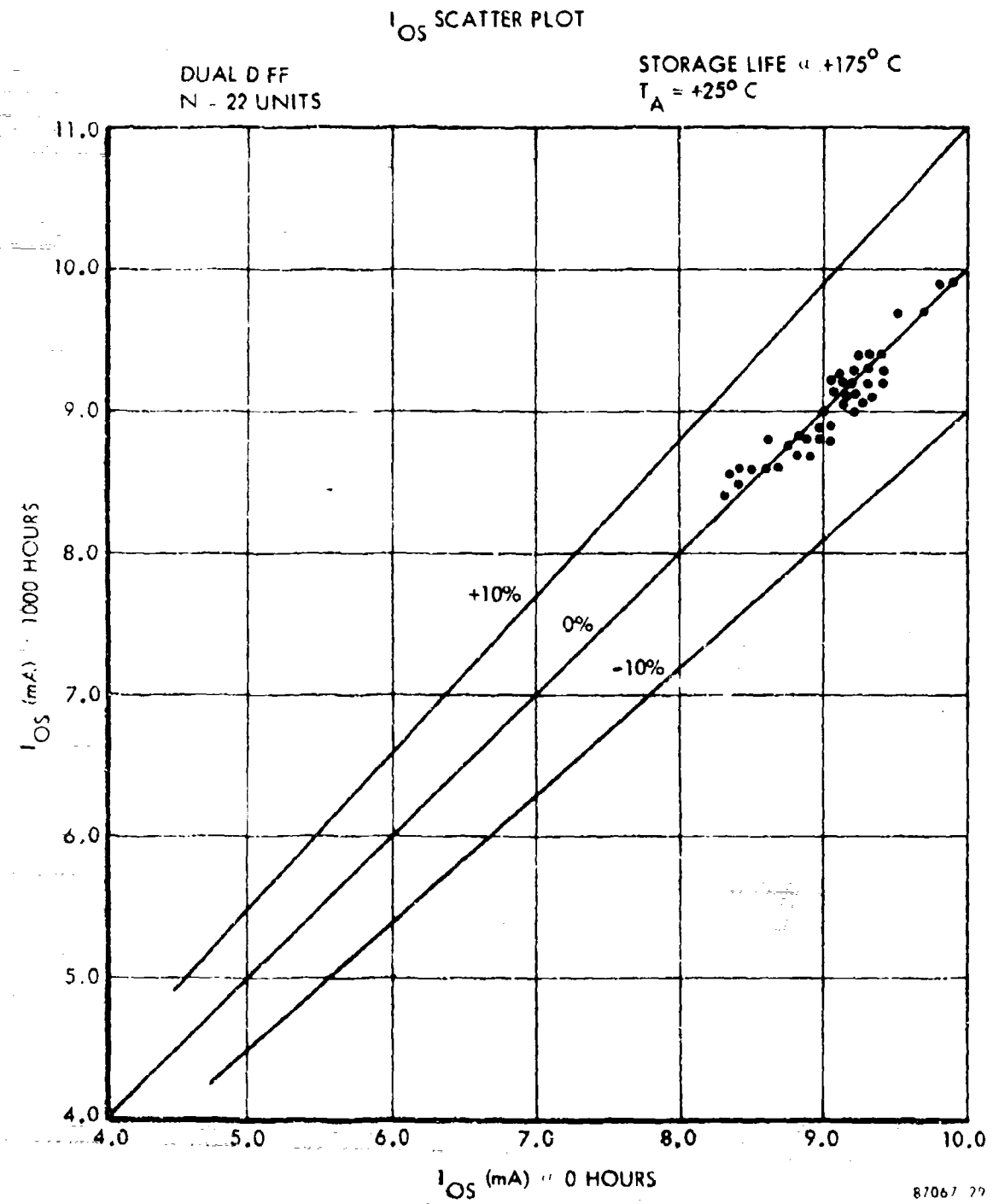


Figure 40. I_{OS} Scatter Plot (Flip-Flop)

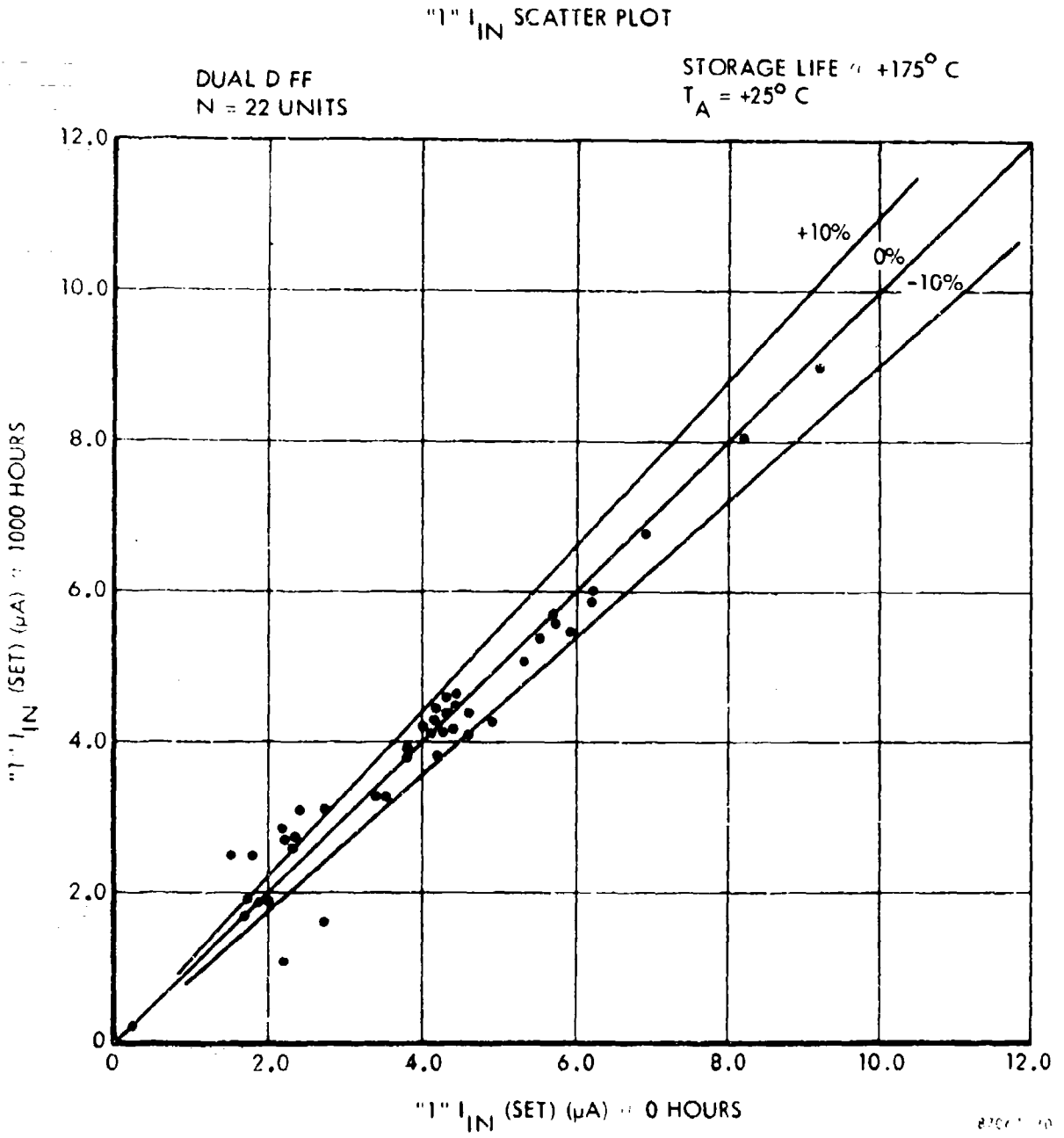


Figure 41. "1" I_{IN} Scatter Plot (Flip-Flop)

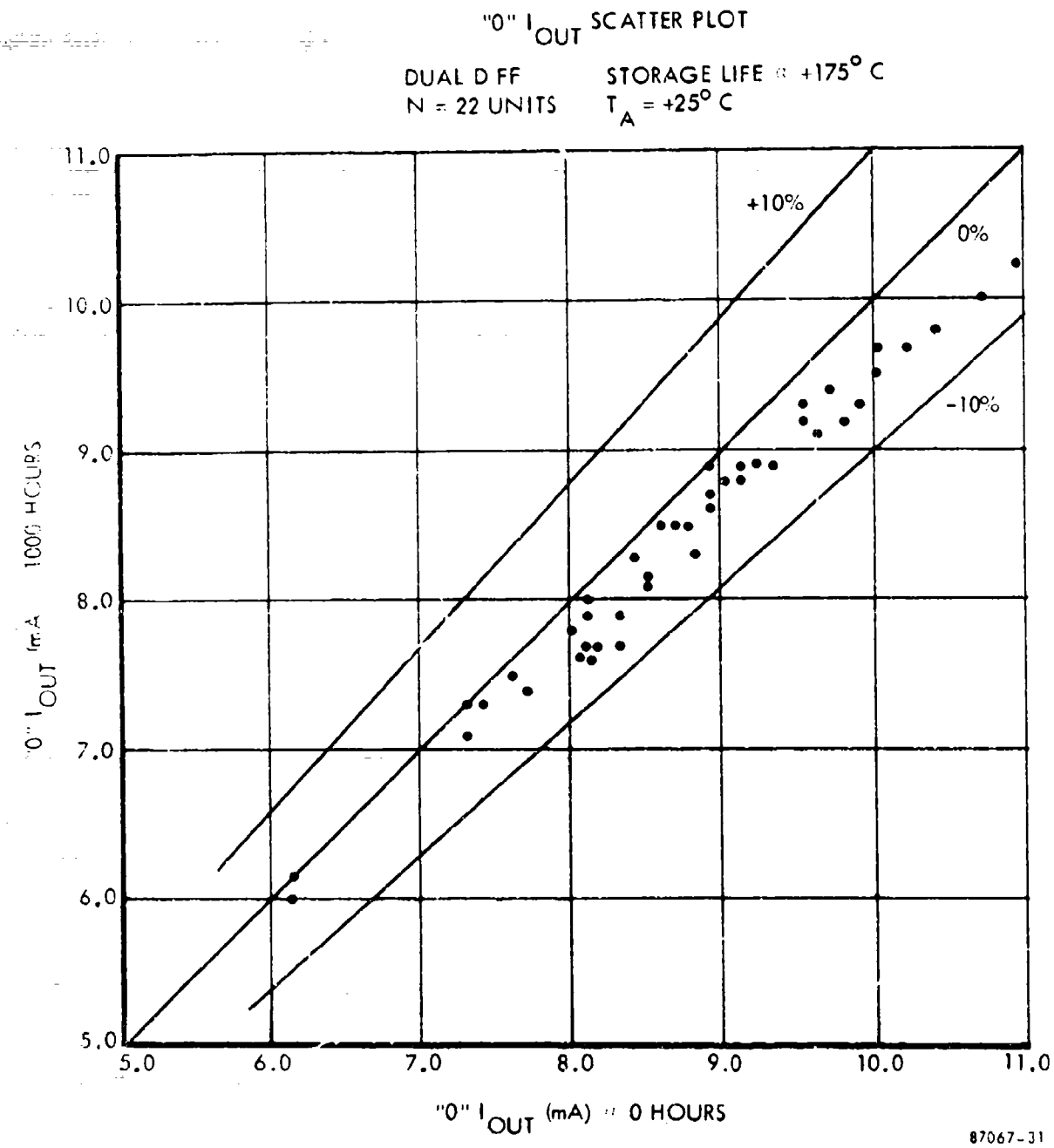


Figure 42. "0" I_{OUT} Scatter Plot (Flip-Flop)

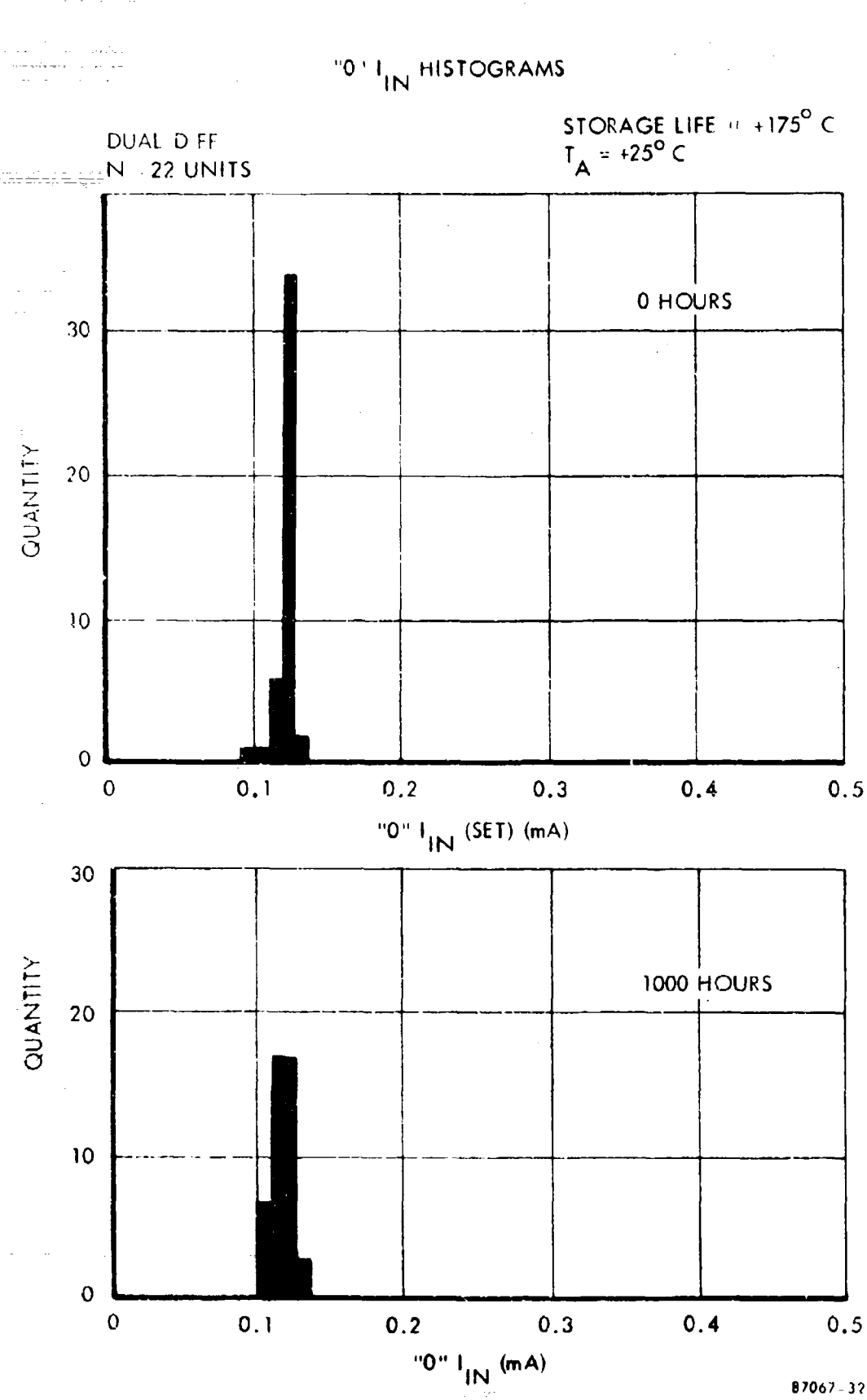


Figure 43. "0" I_{IN} Histograms (Flip-Flop)

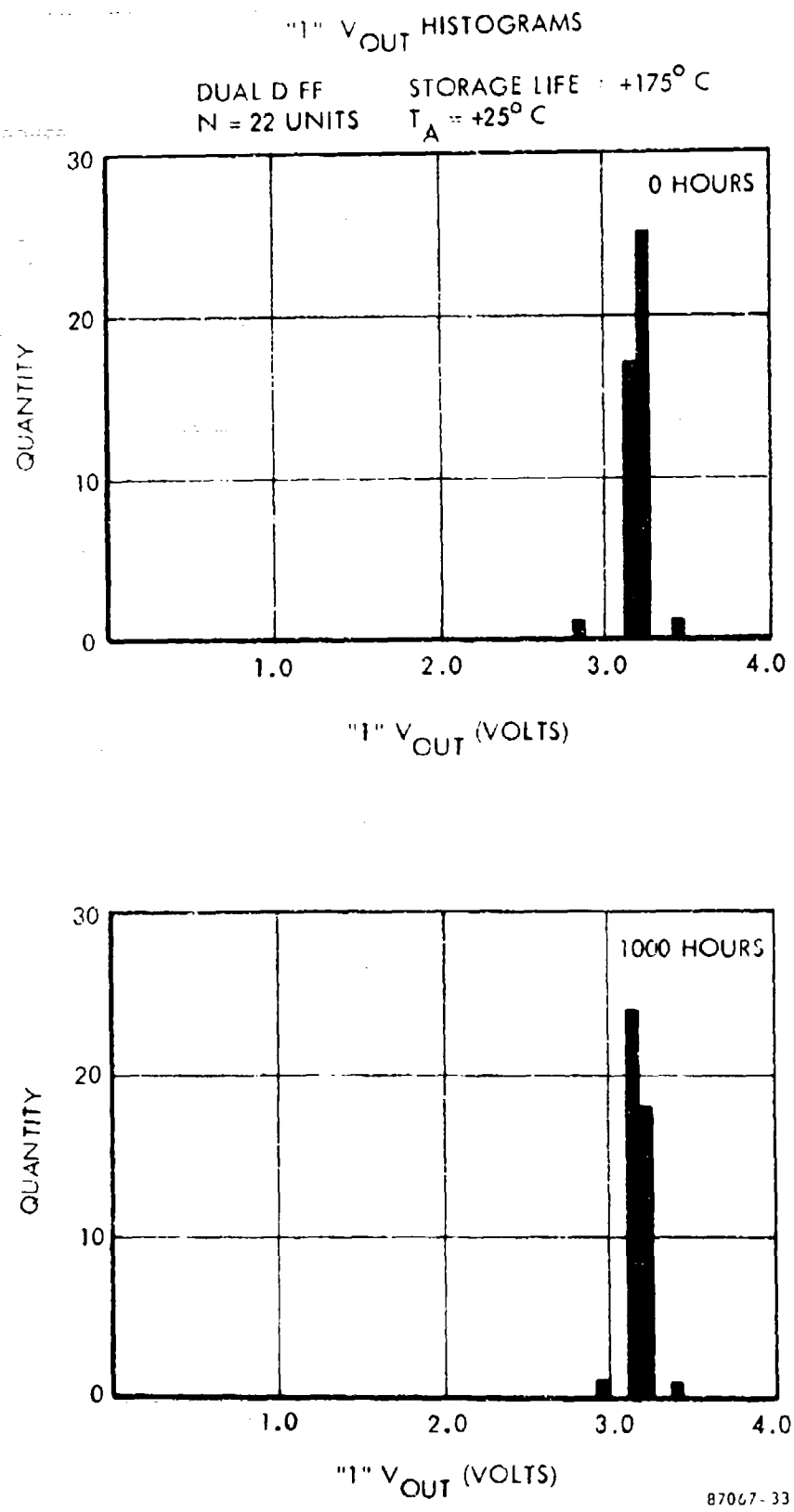


Figure 44. "1" V_{OUT} Histograms (Flip-Flop)

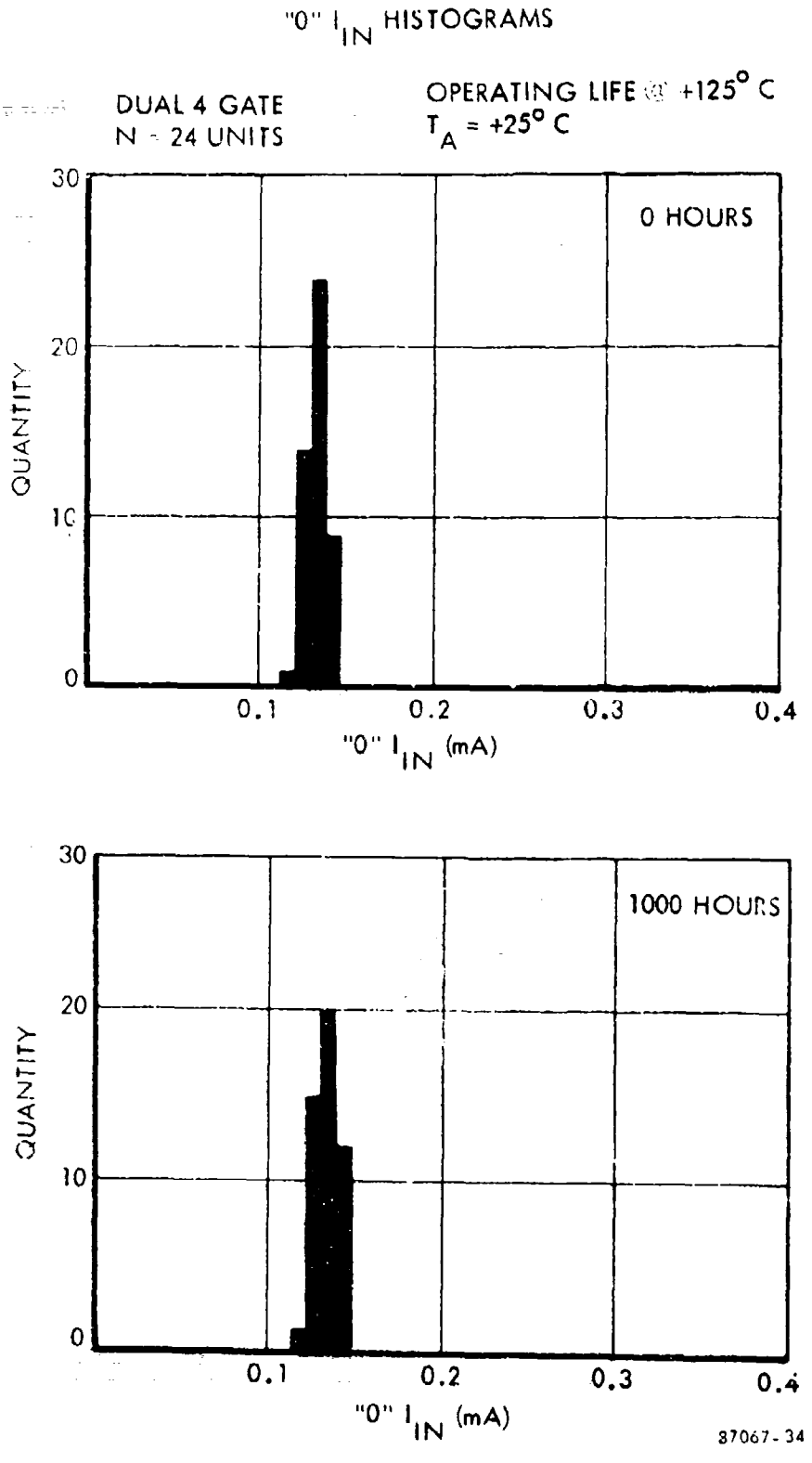


Figure 45. "0" I_{IN} Histograms (Dual 4 Gate)

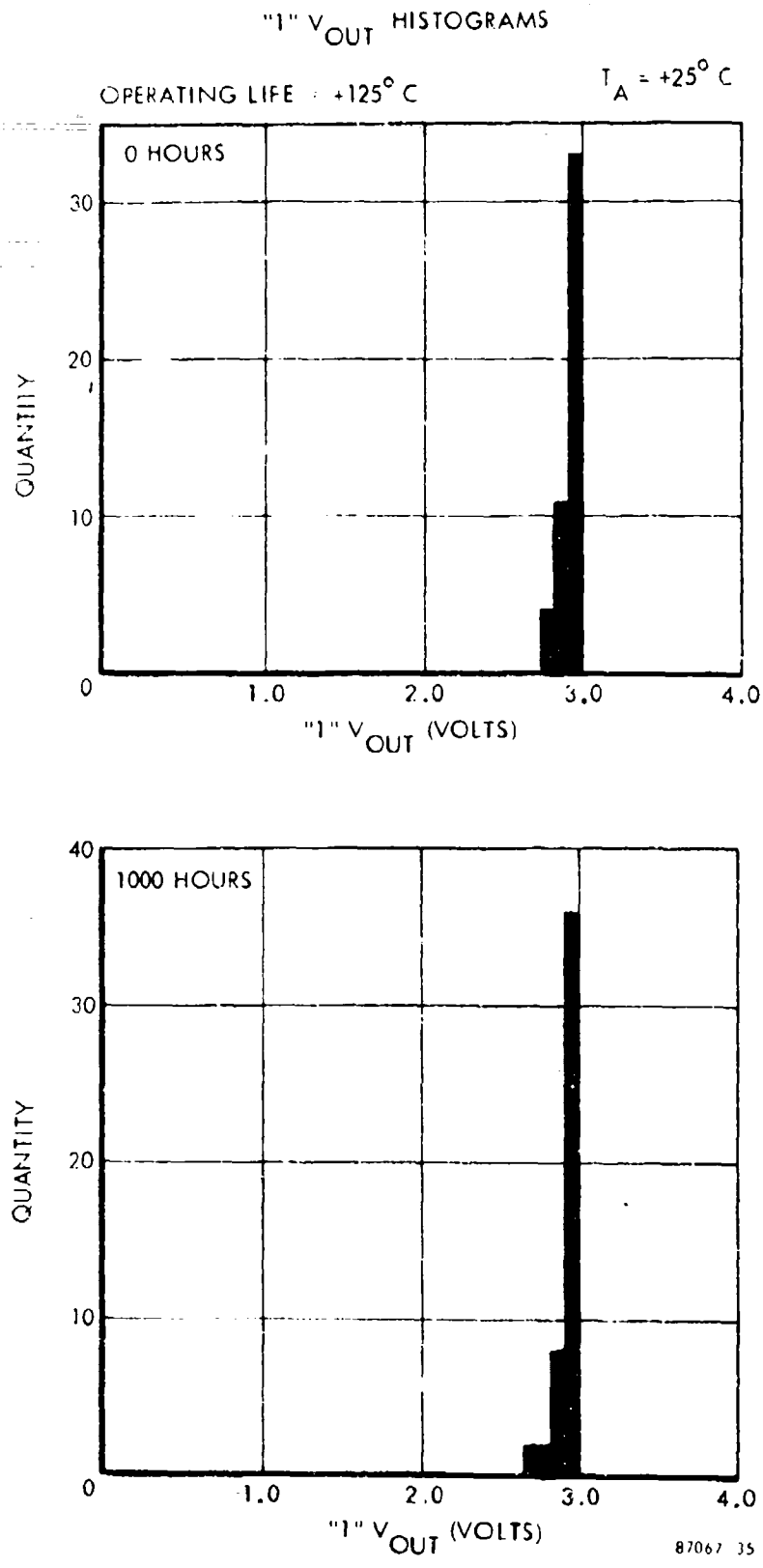


Figure 46. "1" V_{OUT} Histograms (Dual 4 Gate)

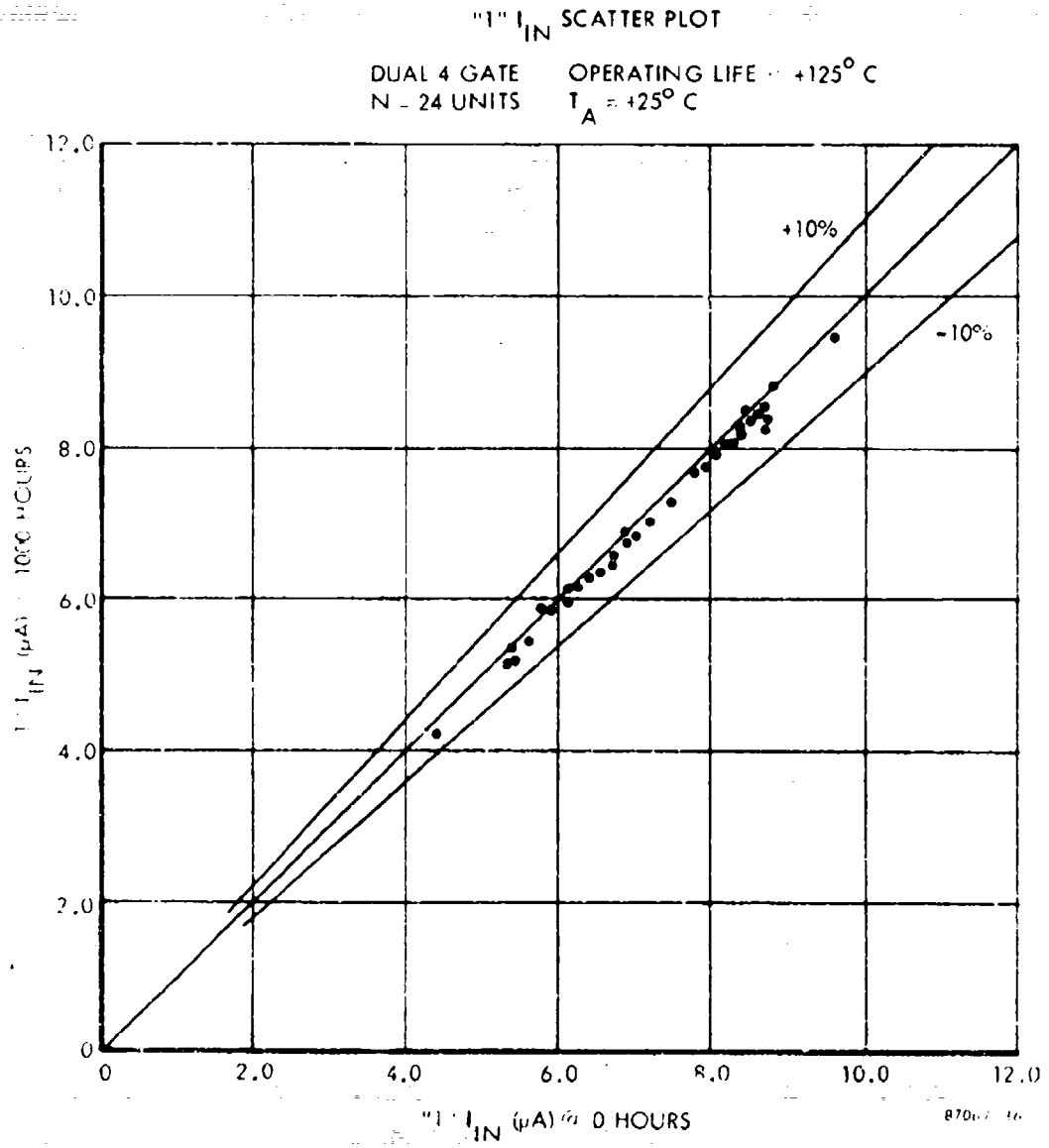


Figure 47. "1" I_{IN} Scatter Plot (Dual 4 Gate)

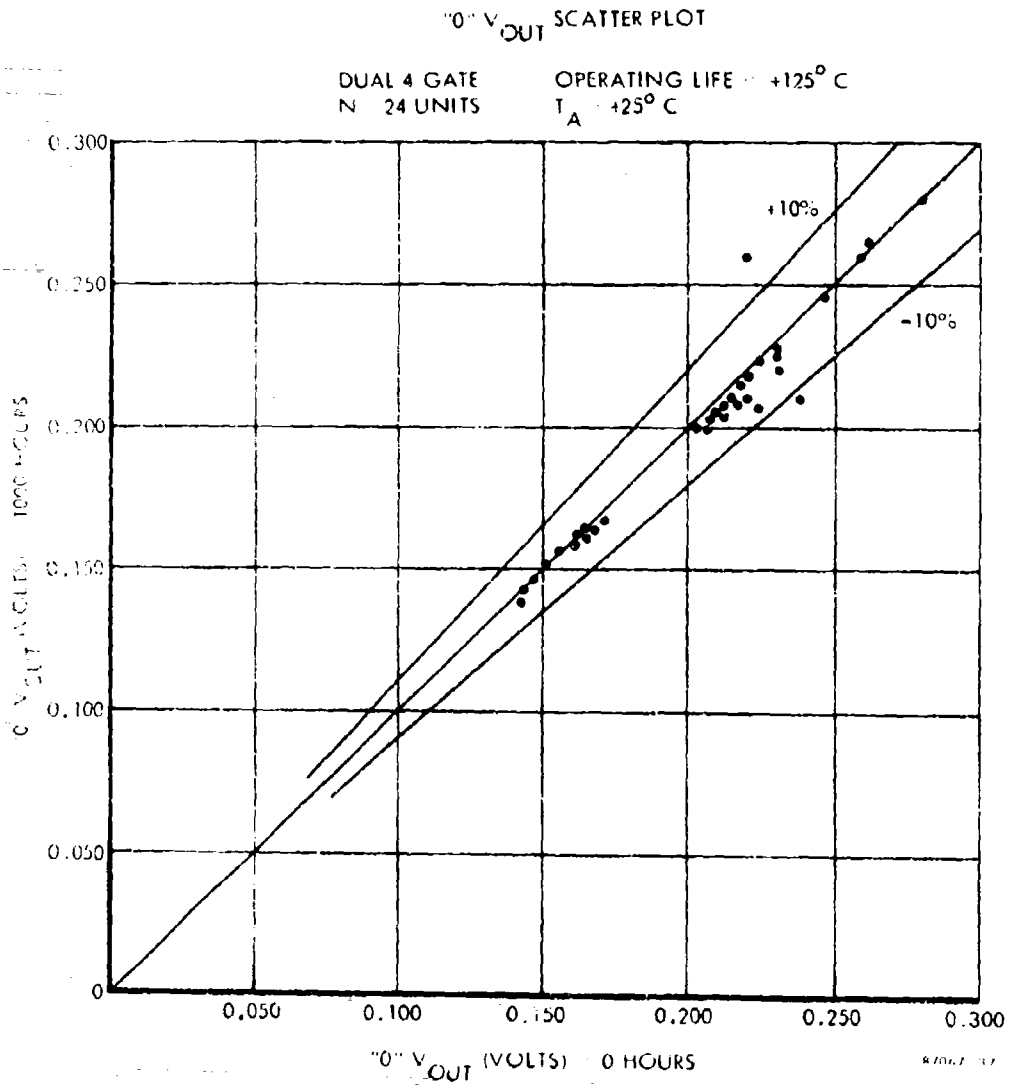


Figure 48. "0" V_{OUT} Scatter Plot (Dual 4 Gate)

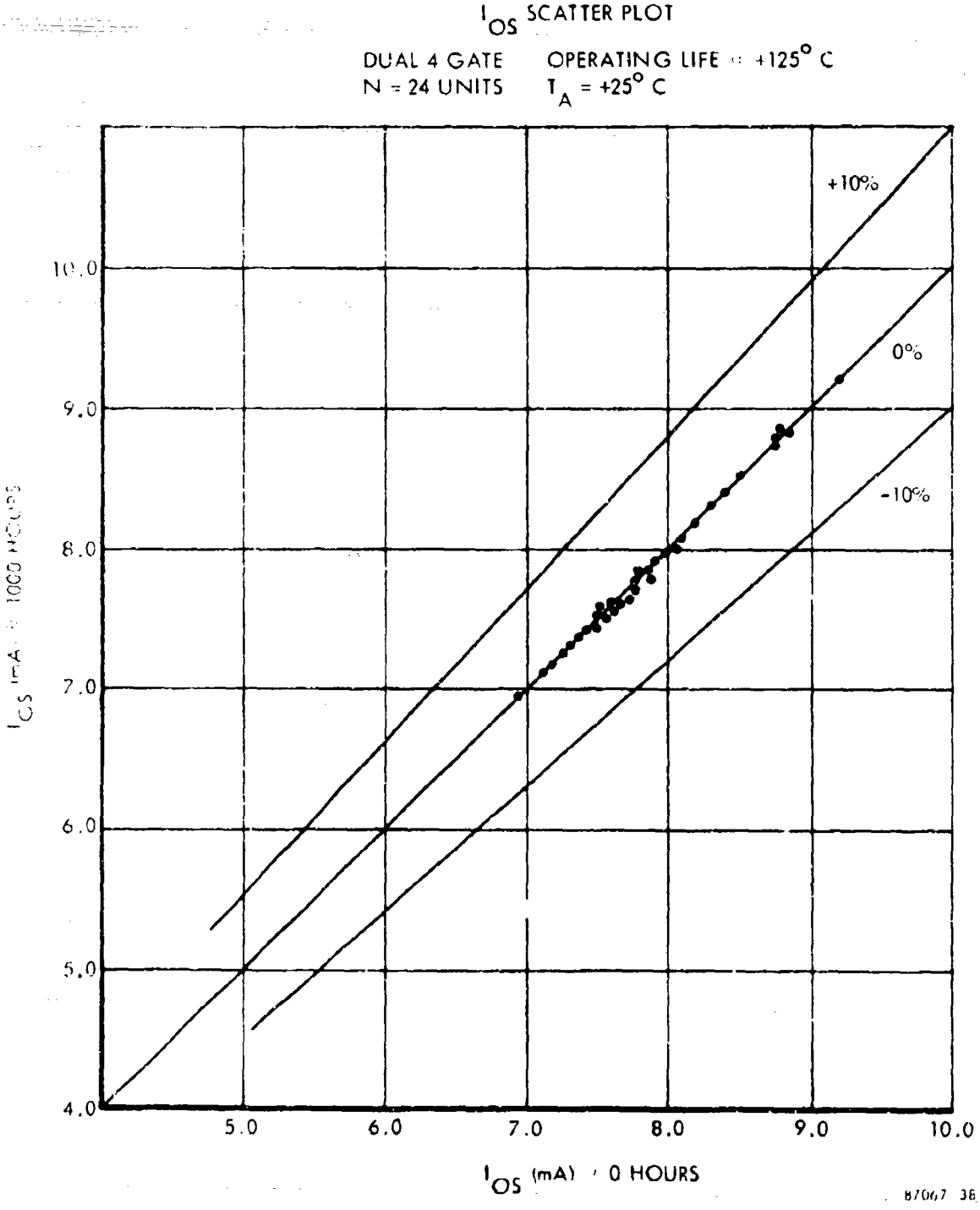


Figure 49. I_{OS} Scatter Plot (Dual 4 Gate)

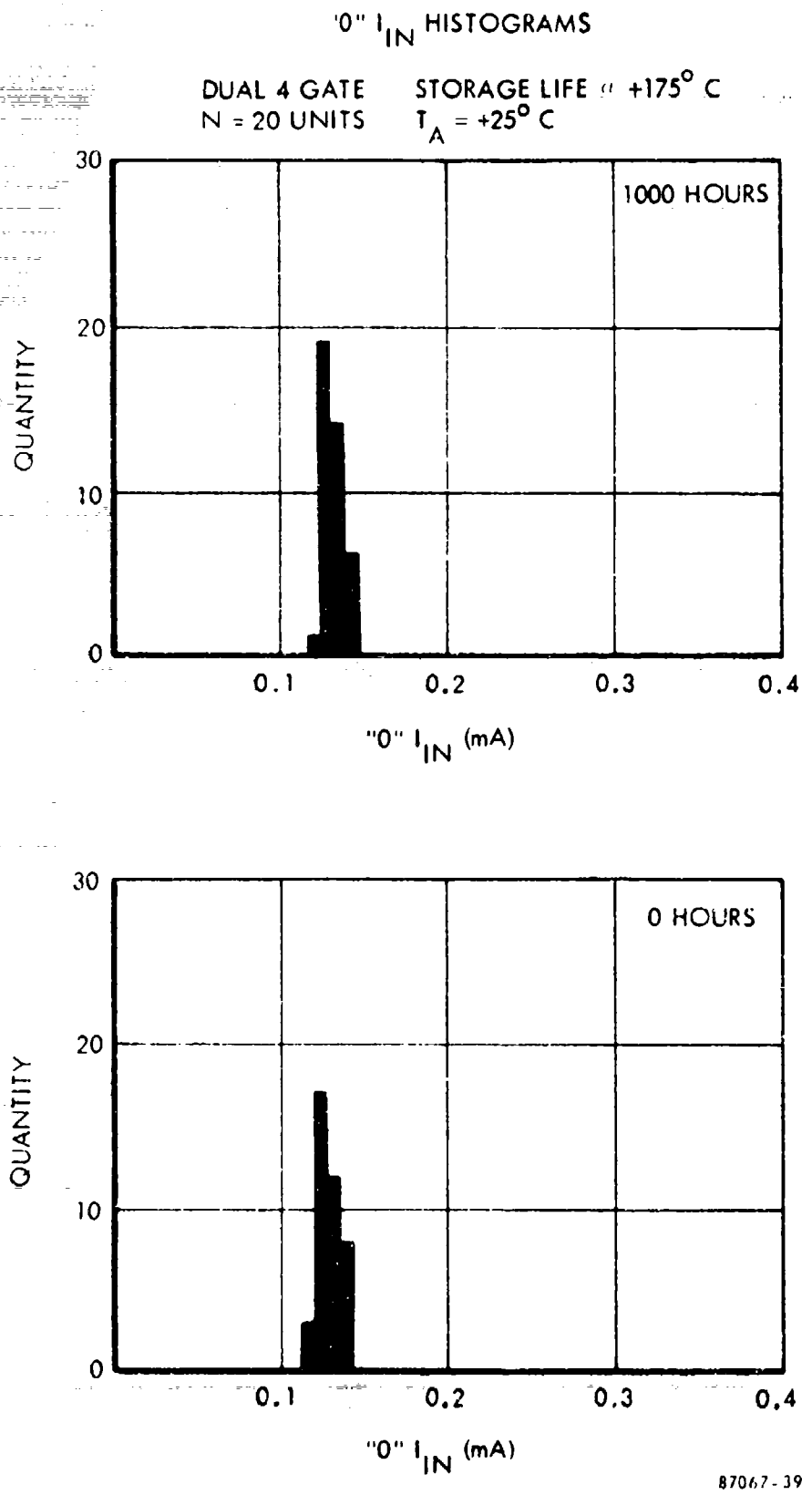


Figure 50. "0" I_{IN} Histograms (Dual 4 Gate)

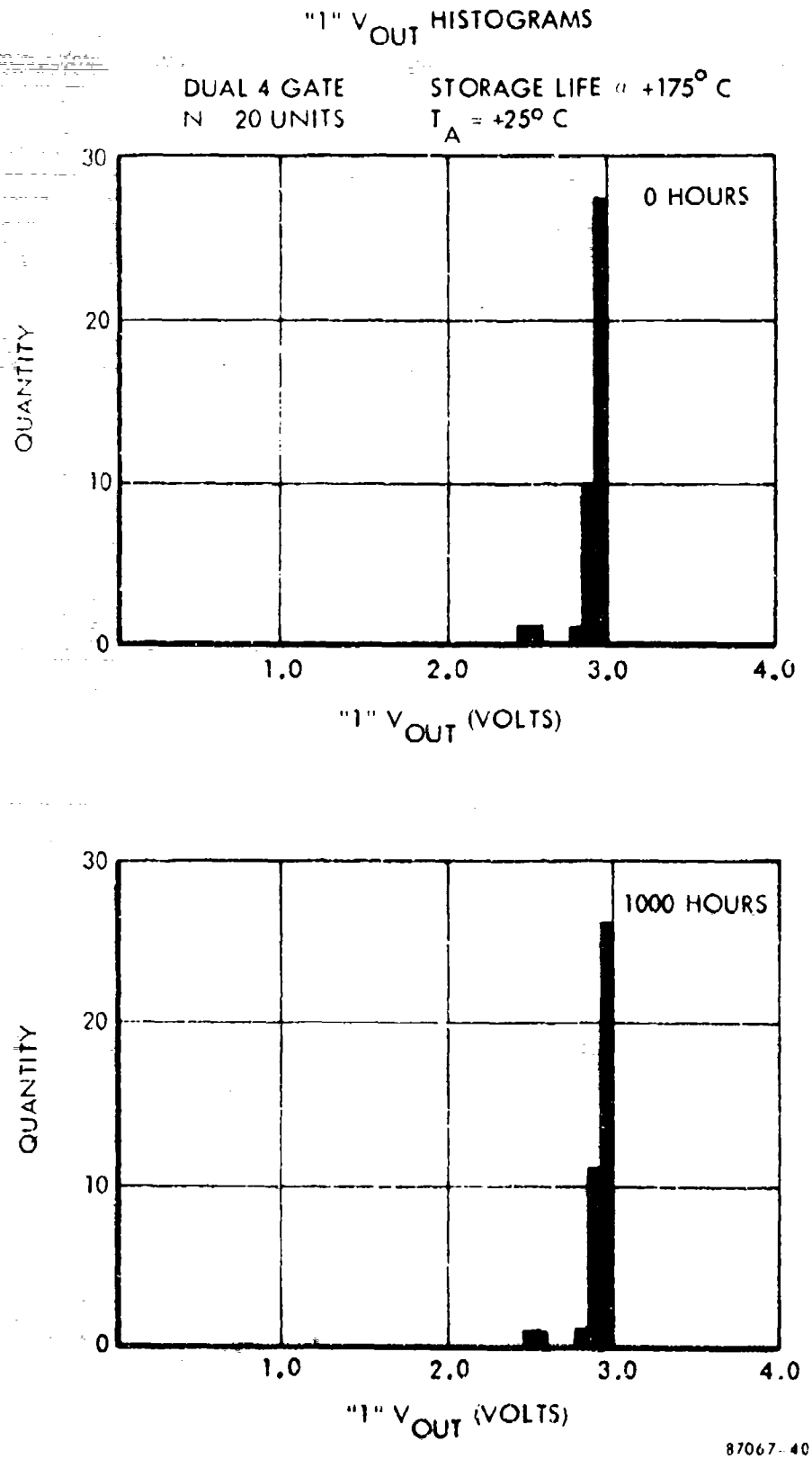


Figure 51. "1" V_{OUT} Histograms (Dual 4 Gate)

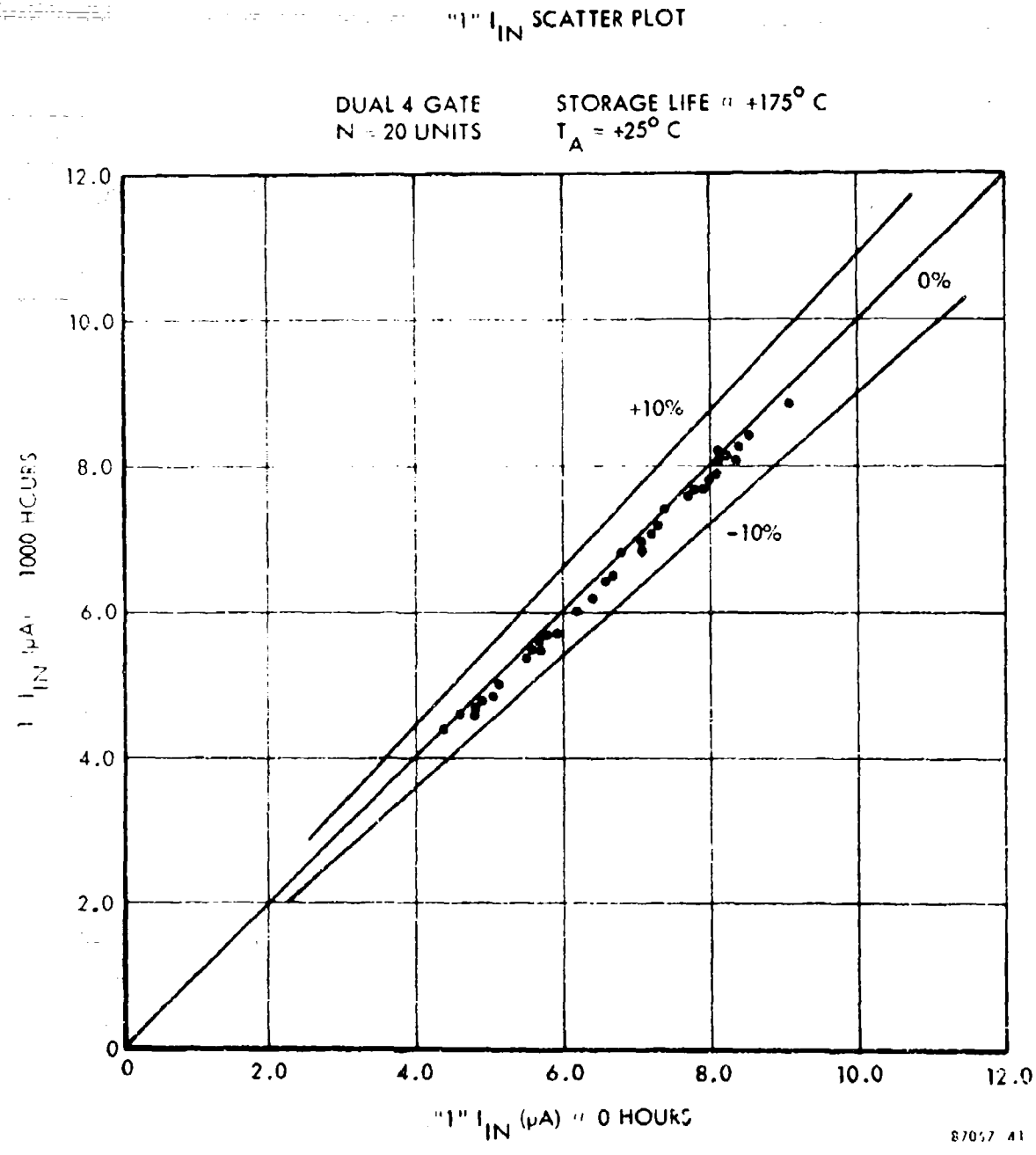


Figure 52. "1" I_{IN} Scatter Plot (Dual 4 Gate)

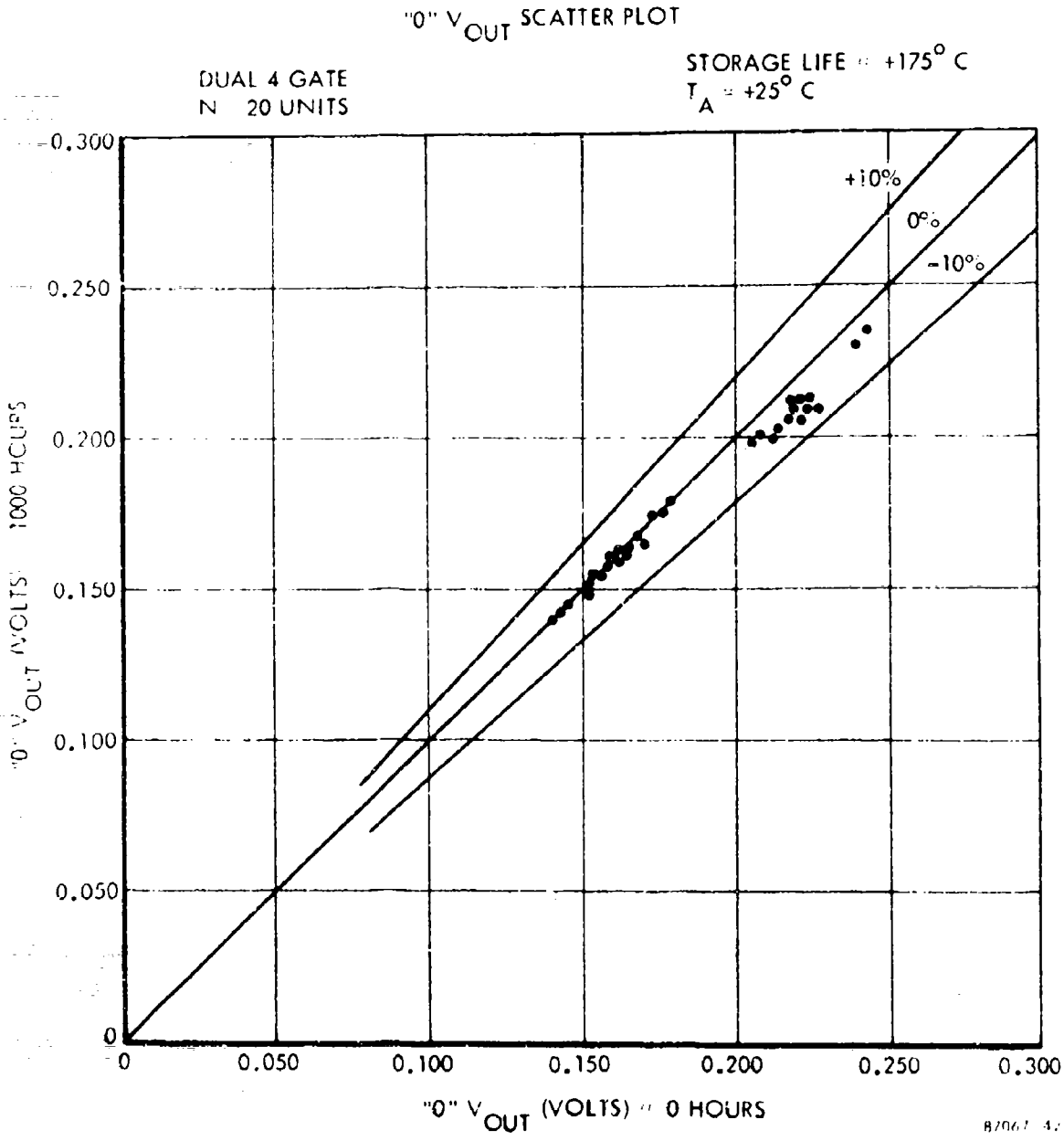


Figure 53. "0" V_{OUT} Scatter Plot (Dual 4 Gate)

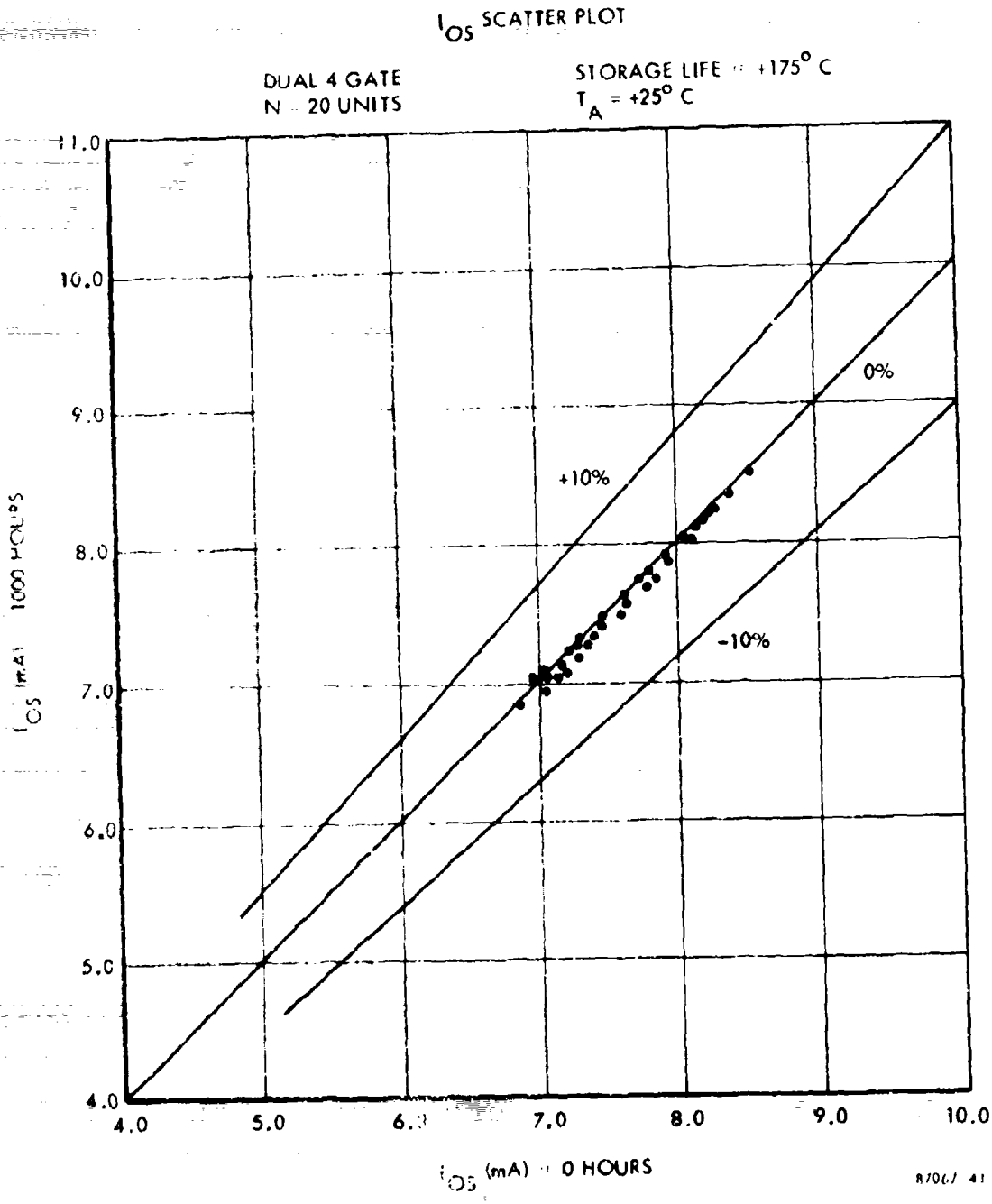


Figure 54. I_{OS} Scatter Plot (Dual 4 Gate)

SECTION VIII

RADIATION HARDNESS

8.0 HARDNESS RESULTS

Both device types produced on this program were exposed to radiation levels of 7×10^{14} neutrons/cm^2. The results obtained indicated superior performance over competitive devices at such environmental levels. Figures 55 through 58 plot the variation of certain key operating parameters of the Dual D Flip-Flop at the various levels of irradiation. Figures 59 through 63 provide plots of similar parameters for the Dual Four Input Gate.

Based on the results obtained, it can be concluded that the device hardness substantially exceeded the design goal set forth in the program requirements.

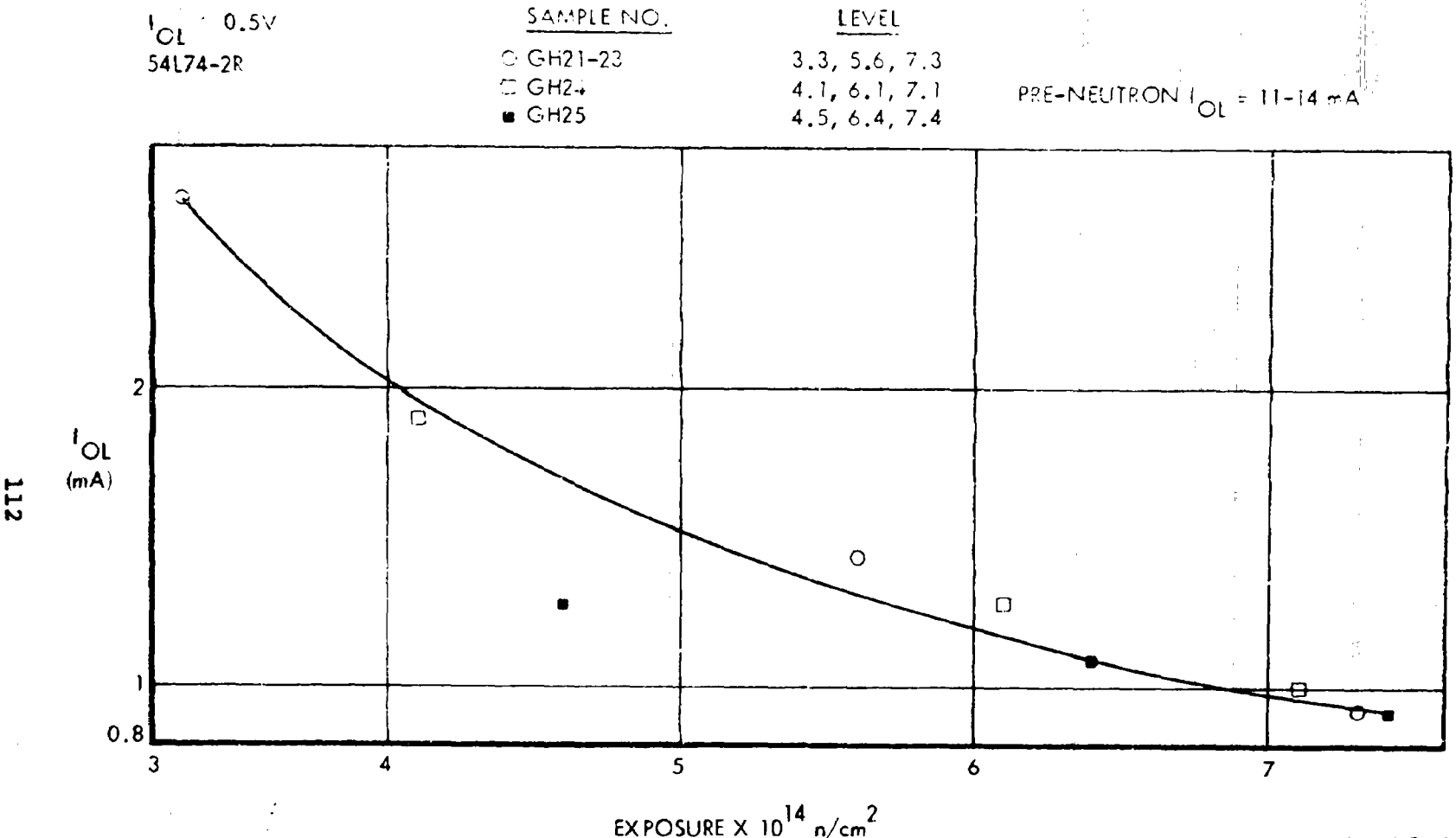


Figure 55. I_{OL} versus Radiation Exposure (Flip-Flop)

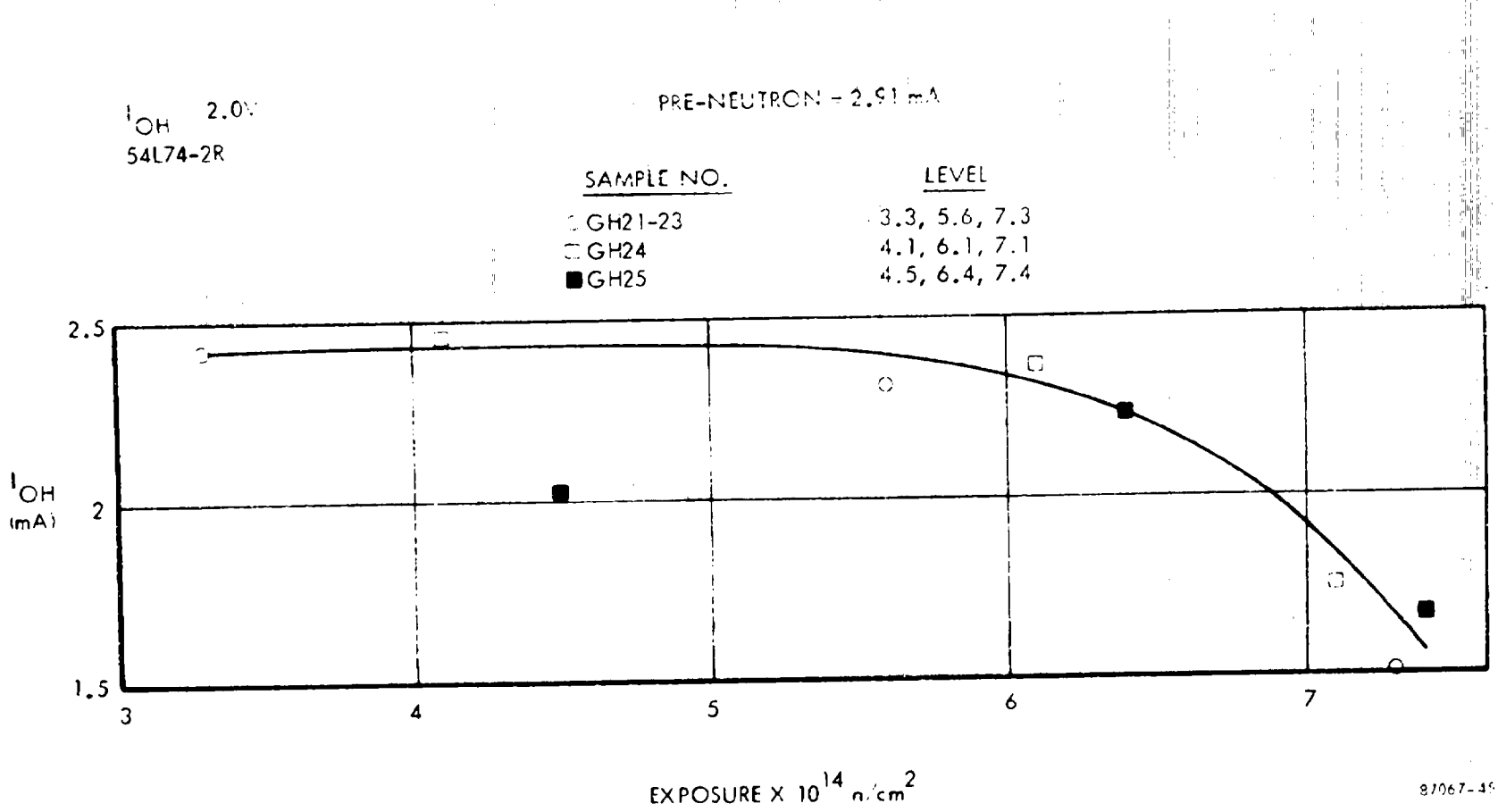


Figure 56. I_{OH} versus Radiation Exposure (Flip-Flop)

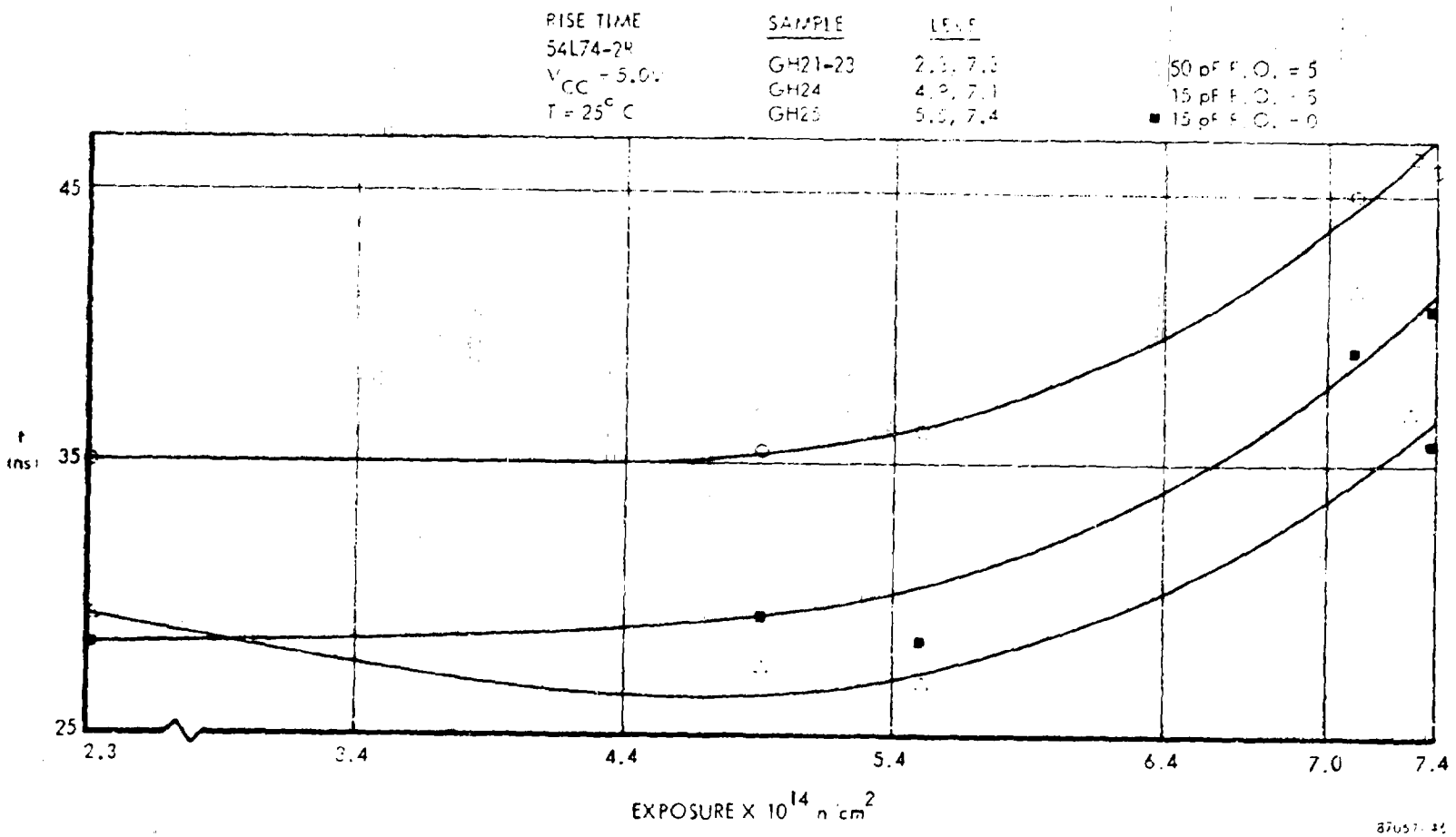


Figure 57. Rise Time versus Radiation Exposure (Flip-Flop)

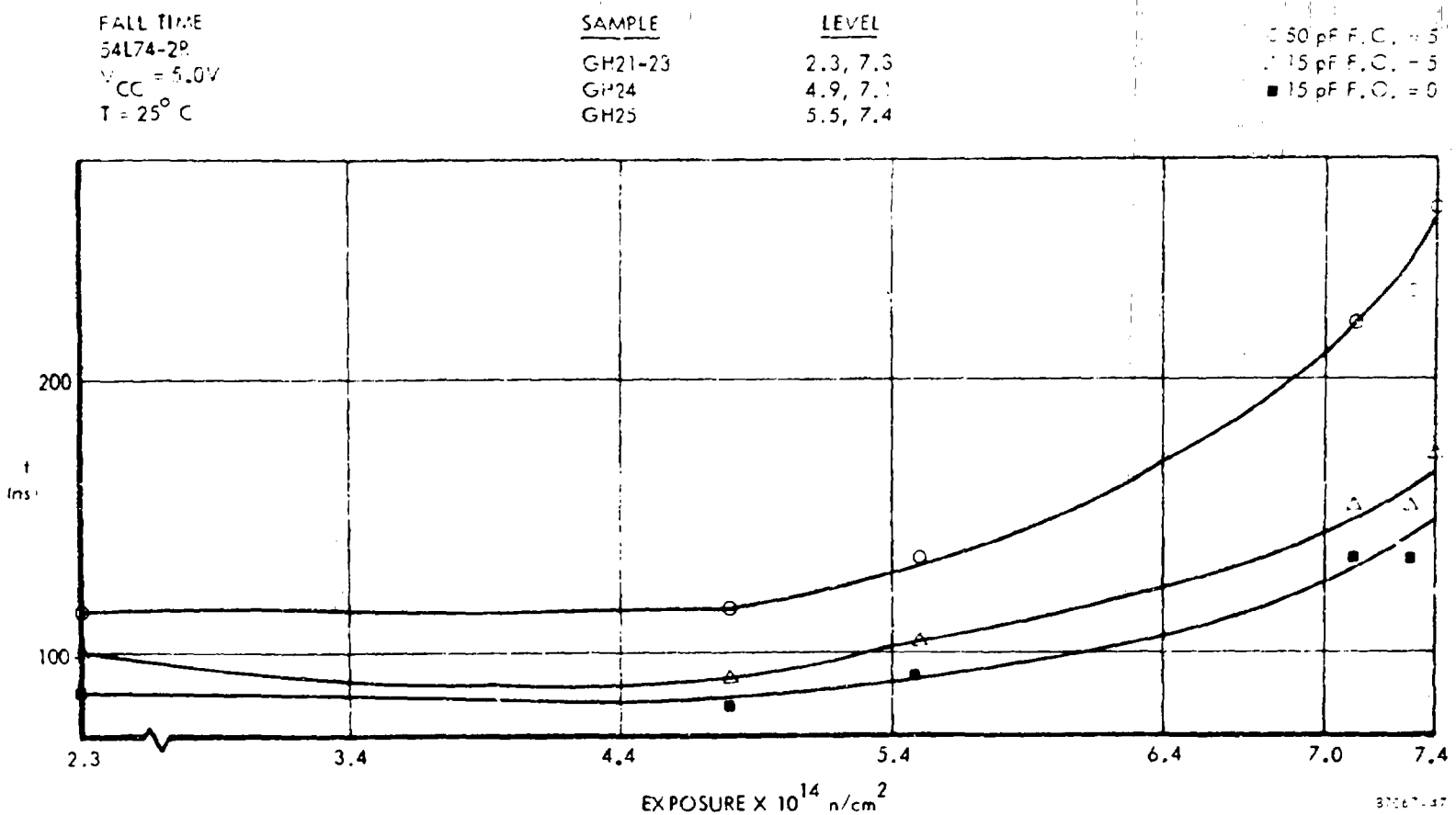


Figure 58. Fall Time versus Radiation Exposure (Flip-Flop)

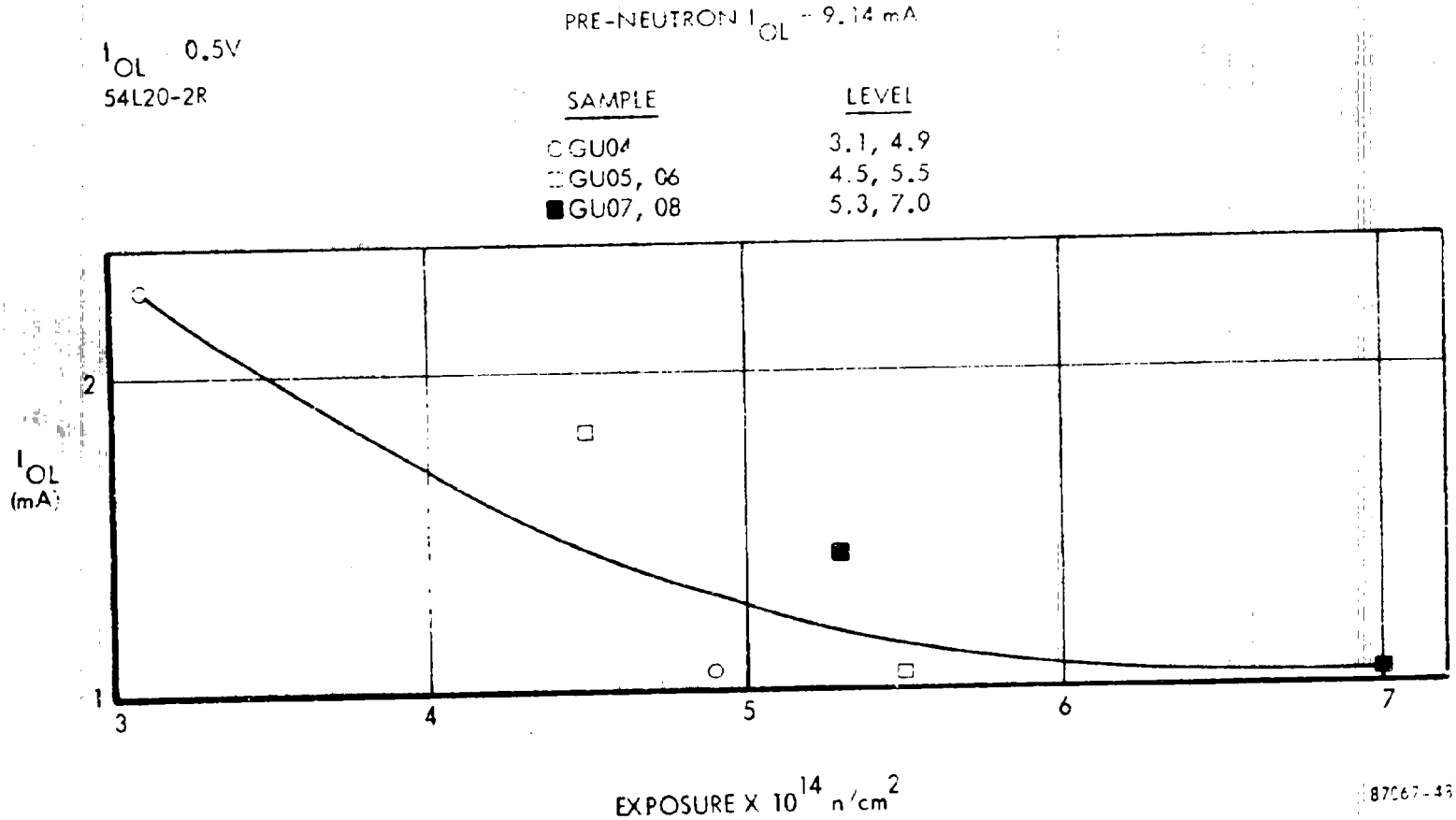


Figure 59. I_{OL} versus Radiation Exposure (Dual 4 Gate)

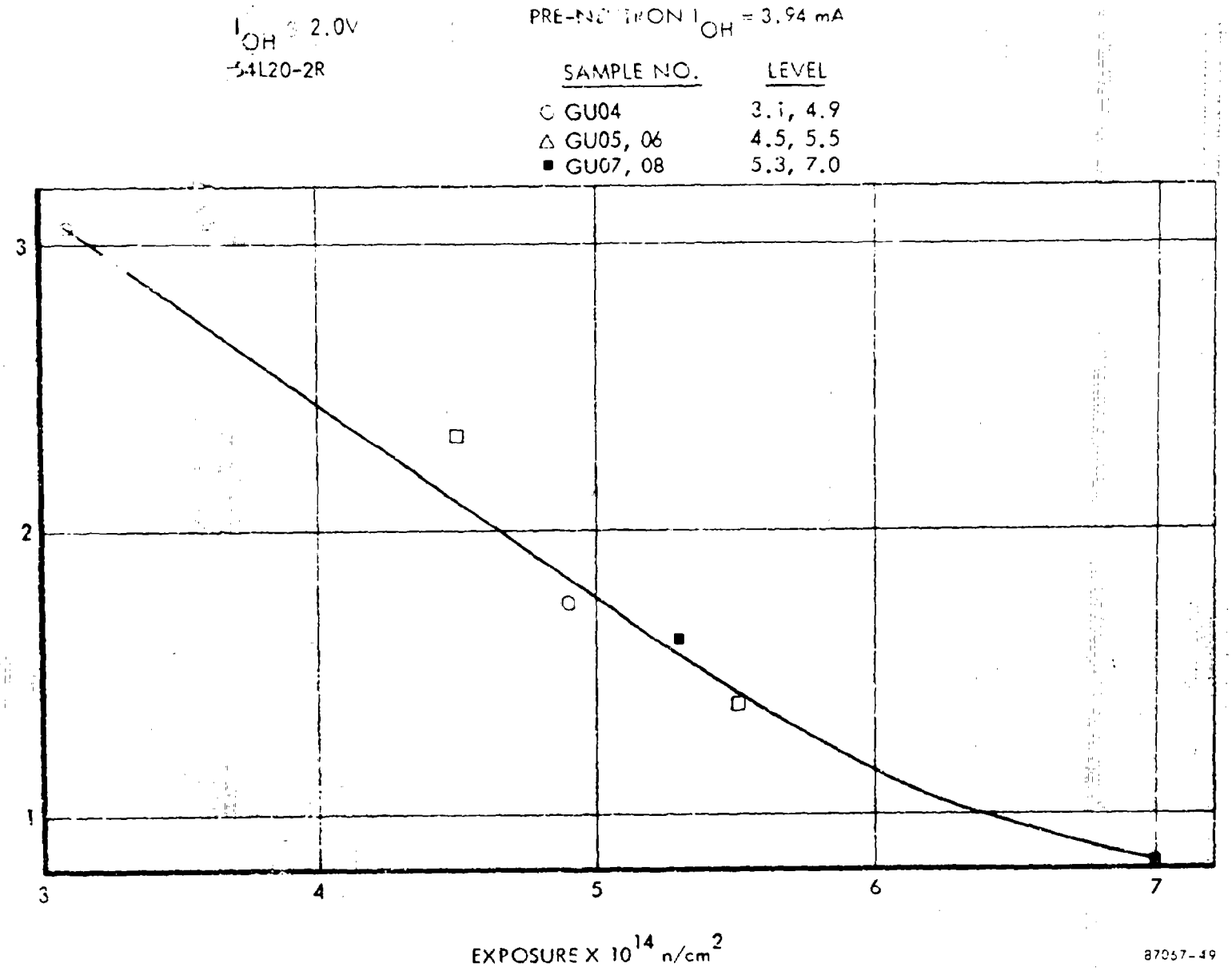


Figure 60. I_{OH} versus Radiation Exposure (Dual 4 Gate)

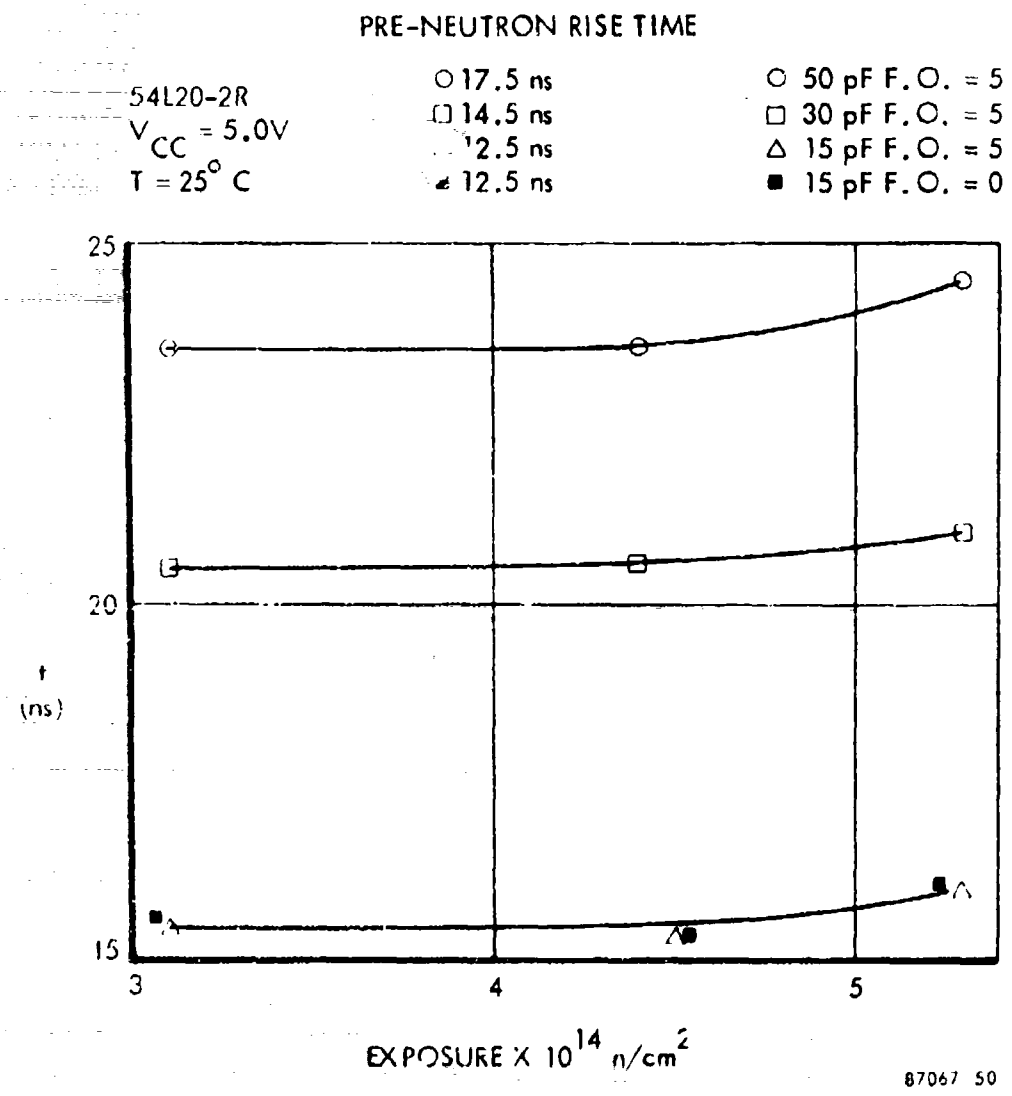


Figure 61. Rise Time versus Radiation Exposure (Dual 4 Gate)

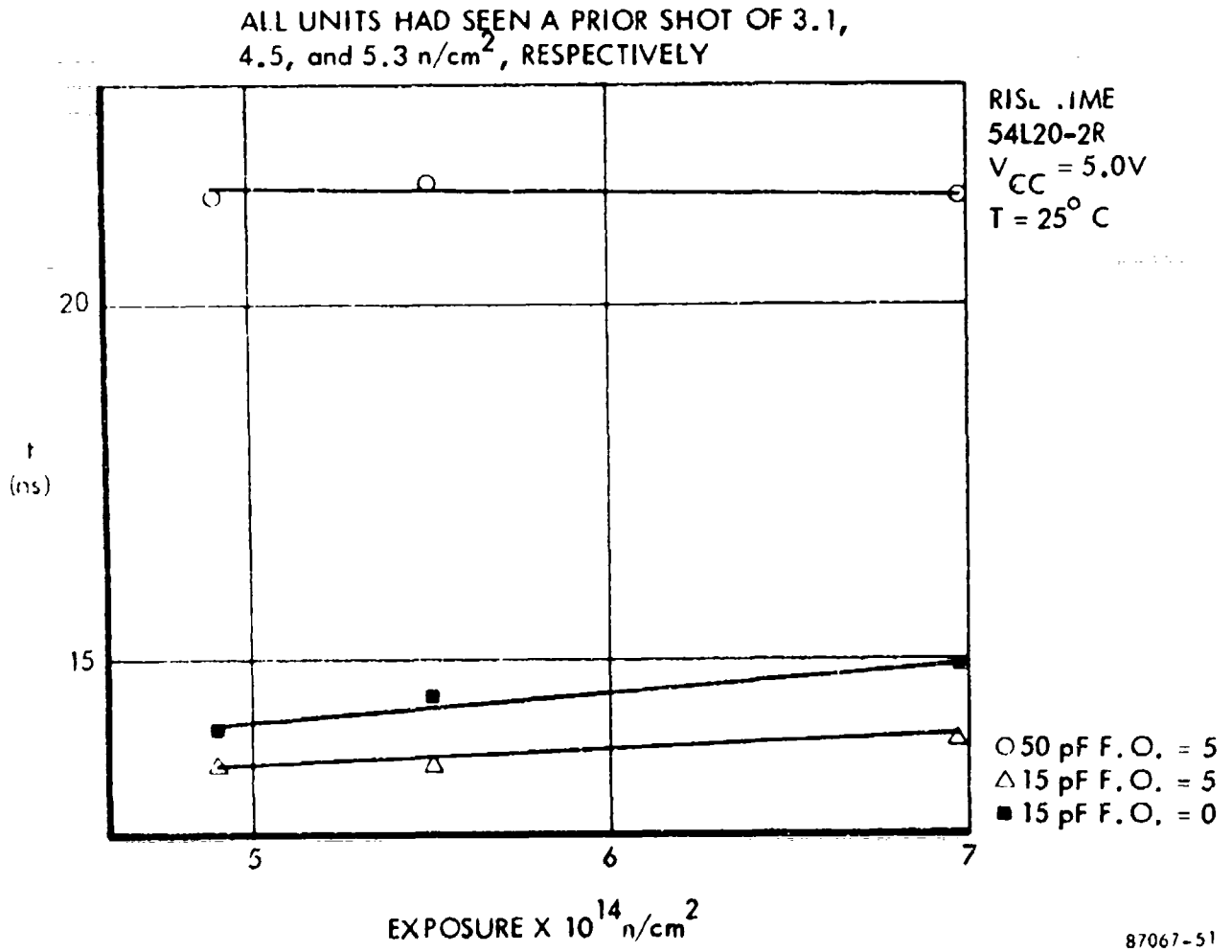


Figure 62. Rise Time versus Radiation Exposure (Dual 4 Gate)

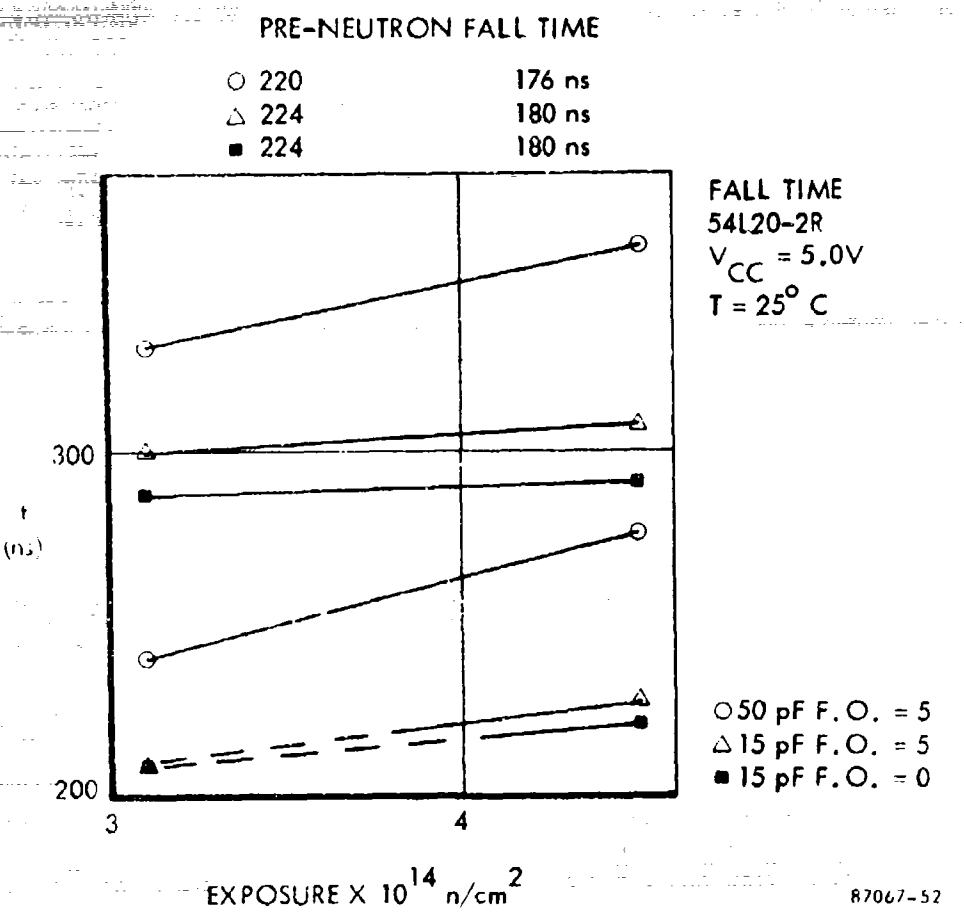


Figure 63. Fall Time versus Radiation Exposure (Dual 4 Gate)

SECTION IX

CONCLUSIONS AND RECOMMENDATIONS

9.0 GENERAL

This section summarizes the conclusions and recommendations of the contract.

9.1 CONCLUSIONS

The project objective to establish the manufacturing processes that are necessary to deploy high resistivity thin film resistors on radiation hardened, low power integrated circuits was achieved. The successful use of AC sputtered chrome silicon (CrSi) resistors in the Series 54 logic configuration was considered sufficient evidence that the sputtered CrSi thin film technology has been successfully developed to be used for the high volume production of a family of similar high reliability devices.

9.1.1 CHROME SILICON RESISTOR TECHNOLOGY

The results of the resistor evaluation allowed the following conclusions to be formulated:

- Resistor linearity was well within the ±1% target specification.
- Resistor tolerances can more than adequately be controlled to tolerances well below the ±20% specified (typically 10 to 15 percent).
- Stability of the chrome silicon resistors is equal to or better than nichrome resistors.
- Stability of the chrome silicon resistors: ΔR drift less than 2 percent/year at 150° C and 100 mW.

9.1.2 SERIES 54L CIRCUIT TECHNOLOGY

Using the chrome silicon resistor technology in the Series 54L logic configurations provided the following conclusions:

- Compatibility exists between silicon dioxide substrate aluminum interconnect and the CrSi resistor process.
- CrSi resistor technology produced logic gates which consumed approximately 1 mW per gate, thus greatly reducing the power requirements for complex systems, when low power and propagation speeds in the order of 50 ns are adquate.

- Chip areas for the 54L devices are approximately 60 percent the size of a compatible 54H type device.

- The wider range of resistor values made possible by the high resistivity material means a broader base of product lines can be considered by the device manufacturers.

9.2 RECOMMENDATIONS

It is recommended that the thin film technology advanced on this project be pursued and applied to system technology requiring the characteristics and specifications of such radiation hardened devices. The basic process technology is applicable to both single level metal as well as multilevel metal.

Harris Semiconductor can manufacture and deliver hardened integrated circuits which use high resistivity films for Air Force missile applications.

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13. ABSTRACT

The principal objective of this program was to advance the processes and techniques that are necessary to add chrome-silicon thin film resistors to radiation hardened, low power integrated circuits. The applicability and repeatability of the resistor deposition techniques using AC sputtered chromium silicide on oxidized silicon were suitable for high volume production.

The following two low power, radiation hardened transistor-transistor logic circuits were fabricated in moderate quantities to demonstrate production readiness of the AC sputtering of thin film resistors for their use in the manufacture of radiation hardened integrated circuits. (1) Dual 3-Input Nand Gate (2) Dual D Type Flip-Flop which includes at least five resistors that have resistance value equal to or greater than 40,000 ohms.

With the successful completion in fabricating six hundred pieces of each device type and the results of severe military environmental tests on these devices, the contract objectives were satisfied.

Some of the technological areas enhanced as a result of the program included development of AC sputtered chrome silicon thin film processing techniques with the following characteristics: Sheet resistivity of 300 to 10K ohms per square, Nominal resistor thicknesses of 200-300A, Stability equal to or greater than nichrome resistors, and Resistor linewidth of 0.5 mil or less.

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